Symmetric Autozeroing Floating-Gate Current Mirror, Differential Pair and Transconductance Amplifier for Ultra Low-Voltage Applications

Yngvar Berg and Mehdi Azadmehr

***Abstract*—In this paper we explore the symmetric autozeroing ultra low-voltage current mirror, differential pair and transconductance amplifier and present some applications. The ultra-low transconductance amplifier has a current boost function and resembles switch-cap and auto-zero circuits. The current boost technique have been used to implement ultra-low voltage digital logic. The simulated data presented is relevant for a $90nm$ TSMC CMOS process.**

***Index Terms*—CMOS, Low-Voltage, Amplifier, Autozero, Differential, Floating-Gate.**

I. Introduction

In this paper we look at the noise properties of ultra-low voltage CMOS transconductance amplifiers. It has always been a challenge to implement analog circuits in a modern digital CMOS process, especially if the analog circuitry is included in a system with clocked digital logic. Traditional amplifiers have been limited by a lower limit for supply voltage given by $2V_t + 2V_{sat}$ which in practice limits the supply voltage close to 1V. Another challenge in mixed signal design is the impact of noise in the supply voltage given by the switching of digital gates. Autozeroing has been proposed as a method to reduce the effect of noise in analog circuits.

While the supply voltage applicable in deep sub-submicron will continue to decrease and eventually fall below $1V$ the threshold voltage will remain relative stable. The gate oxide thickness becomes only a few nanometers and the supply voltage has to be reduced in order to ensure device reliability. In order to maintain maximum dynamic range, a low voltage analog circuit must be able to deal with signal voltages that extend from rail-to-rail. This requires traditional circuit solutions to be replaced by new circuit design strategies.

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) [1]. However, in modern CMOS technologies there are significant gate leakage which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. There are several approaches to FG CMOS logic [2], [3], [4], [5]. The semi floating-gate technique exploited in this paper have been used for digital circuits design [6], [7] and analog design [8].

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In section 2 the basic autozeroing ULV circuit is presented, followed by symmetric ULV transconductance amplifiers in section 3 followed by the conclusion in section 4.

II. Ultra Low-Voltage Circuits

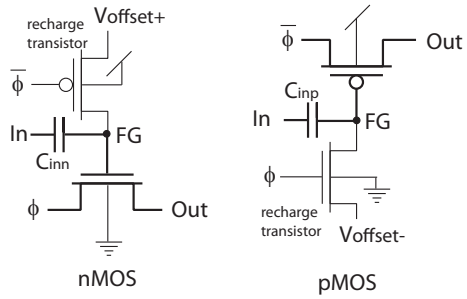

Fig. 1. *MOS and pMOS clocked semi-floating-gate (CSFG) transistors.*

The clocked-semi-floating-gate (CSFG) transistors are shown in Figure 1. The recharge transistors are controlled by clock signals which will force the nMOS evaluate transistor gate terminal (FG) to V_{DD} in the recharge mode, i.e. $\phi = 1$, and the pMOS transistor gate terminal to gnd when recharging. Any input transition will affect the evaluate transistors gate voltage either by a positive or a negative charge. By powering up the gate to source voltages in an initialization phase we are able to reduce the power supply without decreasing the ON current provided by the enhanced transistors. The aim is to maintain a high current level combined with a very low supply voltage. The enhancement can be viewed as an active threshold voltage shift. The recharge transistors are controlled by clock signals which will force the nMOS evaluate transistor gate terminal (FG) to V_{DD} in the recharge mode, i.e. $\phi = 1$, and the pMOS transistor gate terminal to gnd when recharging. Any input transition will affect the evaluate transistors gate voltage either by a positive or a negative charge.

For very low supply voltages the CSFG biasing will not have a significant impact on the current level, and hence neither relative ON nor OFF currents are large. For increasing supply voltages, up to $V_{DD} = V_t$, the relative current increases. For $V_{DD} \leq 0.65Vt$, assuming that $k_{in} \leq 0.7$, where $k_{inn/p} = C_{inn/p}/C_{fg}$ and C_{fg} is the total capacitance seen by the floating gate, the gate to source voltage will never reach the threshold voltage. In this case the transistor will operate in subthreshold regime. The transistors may operate

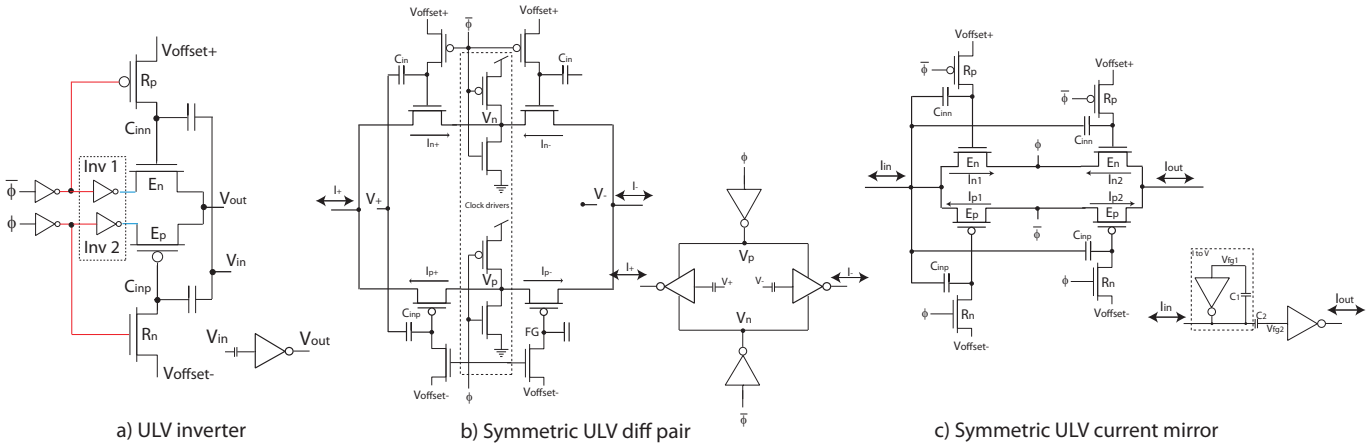

Fig. 2. *a) ULV inverter, b) symmetric ULV differential pair and c) symmetric ULV current mirror.*

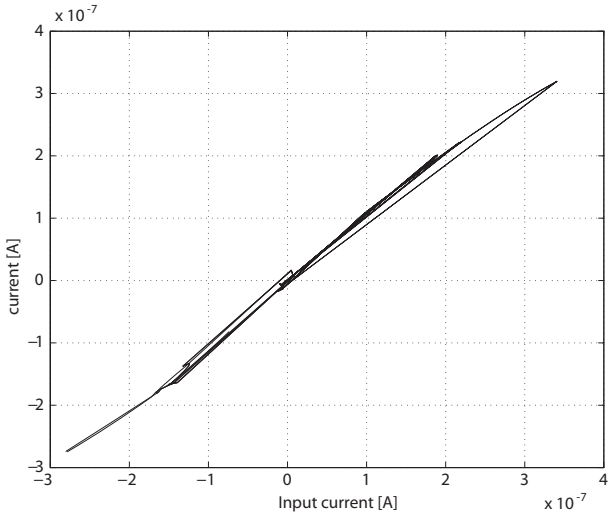

Fig. 3. *The input and output currents of a symmetric current mirror.*

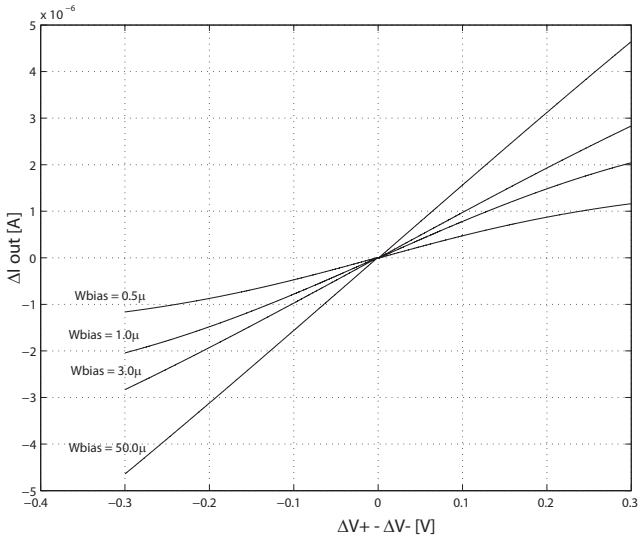

Fig. 4. *The output currents of the symmetric ULV diff pair.* $V_{DD} = 300mV$.

in strong inversion if the supply voltage is close to or above the threshold voltage of the transistors. Furthermore, dummy recharge transistors may be included to reduce noise induced by the clock signal driving the recharge transistor.

The output currents as function of the input currents of the symmetric current mirror[9] are shown in Fig. 3. The bi-directionality of the symmetric current is evident and shows a reasonable linear characteristics and accuracy for a $sine$ input voltage signal producing the input current. The current headroom is $-300nA$ to $300nA$ and the supply voltage is $250mV$.

The output current of the symmetric ULV differential pair[10] is shown in Fig. 4, where the supply voltage is $300mV$ and the offset voltages are $350mV$ and $-50mV$, V_- is swept from $0mV$ to $300mV$ and V_+ is swept from $0V$ to $300mV$, and $W_{bias} = 0.5\mu m$ to $W_{bias} = 50\mu m$. In this case we have used a clock signal of $100MHz$ and an input signal of $200MHz$. As expected the $tanh$ shape of the output current of the differential pair is less evident when the bias transistor including in the clock driver inverters is increased. The degradation of the power supply V_n and V_p is not significant when the width of the bias transistor are very large compared to the minimum sized transistors used in the differential pair. For bias transistor widths exceeding $3\mu m$ the output current is more linear or even slightly $sinh$ shaped when the input capacitors are increased. In that case the differential pair will act as two binary inverters which provide a $sinh$ shaped output current.

A. Autozeroing ULV Gates

A ULV gate including clock drivers is shown in Figure 2. The clock drivers located close to the source/drain terminals of the evaluate transistors may be used to provide current sources. The inverters labeled Inv1 may be used as a bias transistor in a nMOS pseudo differential pair. The effective voltage of the evaluating transistors will be determined by the the supply voltage and the capacitive division associated with the input capacitances.

Both digital and analog ULV circuits can be designed using autozeroing ULV inverters. The clock frequency applied must

be high enough to avoid significant charge leakage during the evaluation phase. The upper limit for the clock frequency depends on the application and input signal frequency. When the gates, i.e. all gates simultaneously, are recharged, hence output precharged to $V_{DD}/2$, the precise output precharge voltage of each gate are adapted to noise relevant for the gate. The precharge voltage is defined by the offset voltages $V_{pre} = (V_{offset+} + V_{offset-})/2$ due to a reverse biasing gate and simple voltage division. If the evaluate transistor are matched, i.e. $V_{offset-} = V_{DD} - V_{offset+}$, the precharge voltage can be expressed as $V_{pre} \approx V_{DD}/2$. Note that the evaluate transistors are not required to be matched accurately, we may adjust the precharge level by using the offset voltages. Assuming that $V_{offset+} = V_{DD}$ and $V_{offset-} = V_{ss} = 0V$ we can estimate the effect of power supply noise on the precharge voltage and accuracy of the autozeroing gate. By modelling the power supply noise as $V_{DD}^{'} = V_{DD} + \Delta V_1$ and $V_{ss}^{'} = 0V + \Delta V_2$ we can express the precharge voltage as $V_{pre} = \left(V_{DD}^{'} + V_{ss}^{'}\right)/2 = (V_{DD} + \Delta V_1 - \Delta V_2)/2$. In addition the nMOS and pMOS evaluate transistors are biased or recharged with the power supply noise ΔV_1 and ΔV_2 respectively. When the gate enters the evaluation phase the gate are biased as an inverter and the power supply noise is evident for the evaluate transistors and the effective gate source voltage of the evaluate transistors, assuming that the precharge voltage is stable, can be expressed as

$$\begin{aligned} V_{DD} + \Delta V_1 - \Delta V_2 \quad & nMOS \\ -(-\Delta V_2 + V_{DD} + \Delta V_1) \quad & pMOS \\ = -(V_{DD} + \Delta V_1 - \Delta V_2) \quad & , \end{aligned} \tag{1}$$

and the evaluate transistors remain matched after the autozeroing is performed. All ULV gates respond only to AC signals and blocks the DC level of input signals. This means that the precharge level of inputs and outputs are not important for the circuit's functionality and accuracy. This feature makes it easier to use ULV circuits together with other subsystems with different supply voltages and you can use external input signals with any DC level.

The switching of power supply when entering the evaluate mode may affect the accuracy of the ULV gate if there is an inherent mismatch associated with the avaluate transistors. This mismatch is not affected by power supply noise or other forms of circuit noise. Transistor mismatches, however may affect the operation of the ULV gates. Ideally the precharge voltage should $V_{DD}/2$, or $(V_{DD} + \Delta V_1 - \Delta V_2)/2$ in the presence of power supply noise. Evaluate transistor mismatch will affect the out precharge directly through the voltage diviasion in recharge mode. By modelling the mismatch as a transistor threshold voltage shift of the nMOS evaluate transistor, i.e. $V_{pre} = V_{tn} = V_{tn_nominal} + \Delta V_3$, the precharge voltage will be $V_{pre} = (V_{DD} + \Delta V_1 - \Delta V_2 + \Delta V_3)/2$. When the circuit enters the evaluate mode the output voltage of the gate will be pulled towards one of the rails depending on the sign of ΔV_3. If $\Delta V_3 < 0$ the nMOS is weak and the ouput will be pulled towards V_{ss} and the AC effect of parasitic capacitance seen from the output and to the semi floating-gates C_{sg} (and eventually C_{dg}) will increase the effective threshold voltage of the nMOS evaluate transistor and reduce the effective threshold voltage of the pMOS evaluate transistors assocoated with the gate. Hence, the autozeriong will reduce the affect of transistor mismatces locally. The prceding gate may, however also be affected by the transisor mismatches of a gate. If the precharge level of a specific gate is lower than $V_{DD}/2$ due to a strong nMOS evaluate transistor the precharge level of a following circuit will be higher than $V_{DD}/2$ and so on. A chain of gates will perform a global common autozero, ie.e with all inherent transistor mismatches, with local autozero and slighly different precharge voltages.

III. Symmetric ULV Transconductance Amplifier

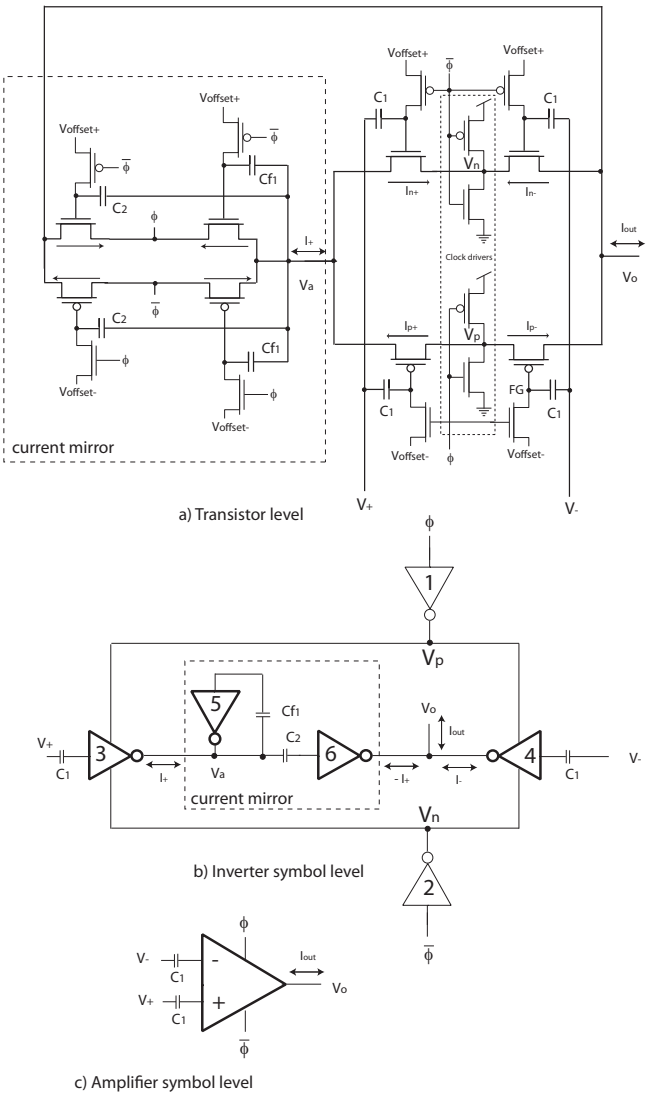

Fig. 5. *ULV transconductance amplifier.*

The ULV transconductance amplifier is shown in Figure 5. Transistor level shown in Figure 5 a) consists of a bidirectional pseudo differential pair and a bidirectional cirrent mirror. We may use simplified ULV inverter symbols for the amplifier as shown in Figure 5 b) where the clock drivers provind

the tail current for the pseudo differential pairs are labeled 1 and 2 and the inverters labeled 3 and 4 are the differential input stage of the bidirectional differential pair. The inverters labeled 5 and 6 provide for the current mirror function. The amplifier level symbol is shown in Figure 5 c). Inverter 5 and the local feedback capacitor C_{f1} converts the output current I_+ of inverter 3 to a voltage $V_a = V_{DD} - V_+$ which yields an output current of the current mirror, i.e. inverter 6, equal to $-I_+$.

A significant feature of the symmetrical circuits results in increased transconductance. Basically, after recharge the currents i_{n+} and i_{p+} and i_n and i_p, will be the same. Any change in the differential input $\Delta V_{in} = \Delta V_+ - \Delta V_-$ will produce a change in all currents so that

$$\begin{aligned} \Delta I_{n+} &= -\Delta I_{n-} \\ &= -\Delta I_{p+} \\ &= \Delta I_{p-} \\ I_+ &= \Delta I_{p+} - \Delta I_{n+} \\ I_- &= \Delta I_{p-} - \Delta I_{n-} \\ I_+ &= -I_-, \end{aligned}$$

and the transconductance of the symmetric pseudo-differential pair is thus the sum of the transconductance of each of the differential pair.

The autozeroing of the ULV gates is performed on the inverter level shown in Figure 5 c) where inverters 5 and 6 are directly connected to virtual power supply provided by clock drivers.

Inverters 3 and 4 however perform autozeroing when connected to virtual power $V_p = V'_{DD}$ and $V_n = V'_{ss}$. The floating gates are recharged to V_{DD}, and V'_{ss} in the recharge phase and when entering the evaluate phase the effective gate to source voltages of the bias transistors are equal to $V_{DD} - V_{ss'}$ and $-V'_{DD}$ for the nMOS and pMOS pseudo differential pair respectively. Furthermore the evaluate transistors of inverters 3 and 4 which form the symmetric differential pair will be recharged to $V'_{DD} - V'_n$ and $V'_p - V'_{ss}$. The condition $I_{n+} = I_{n-}$ and $I_{p+} = I_{p-}$ still holds, $I_{n+} = I_{p+}$ and $I_{n-} = I_{p-}$ must be satisfied. Assume a positive ΔV_1, i.e. $V'_{DD} = V_{DD} + \Delta V_1$, the nMOS evaluate transistor will be recharged to provide more current than the pMOS counterparts. In the evaluate mode the increased power supply will increase the current level of the pMOS evaluate transistor and the increased current of the nMOS evaluate tyransistors will be matched. Furthermore, the current level will match the current level of the symmetric current mirrors as well. In fact, all symmetric ULV gates will be adjusted to the specific power supply available when the circuits enters the recharge state. The autozeroing or recharge frequency may be choosen i a wide range to avoid supply noise and noise imposed by leakage. Note, that the autozeroing is performed at all nodes driven including the internal node V_a in the amplifier shown in Figure 5.

The ULV gates are noise tolerant due to two major aspects

1) **Symmetry.** All ULV gates, both analog and digital, are symmetric. The symmetry allows any circuit to be connected to any other circuit without considering the dc level.
2) **Autozeroing.** All ULV gates, both analog and digital, perform autoaeroing at a high rate to reduce impact of noise.

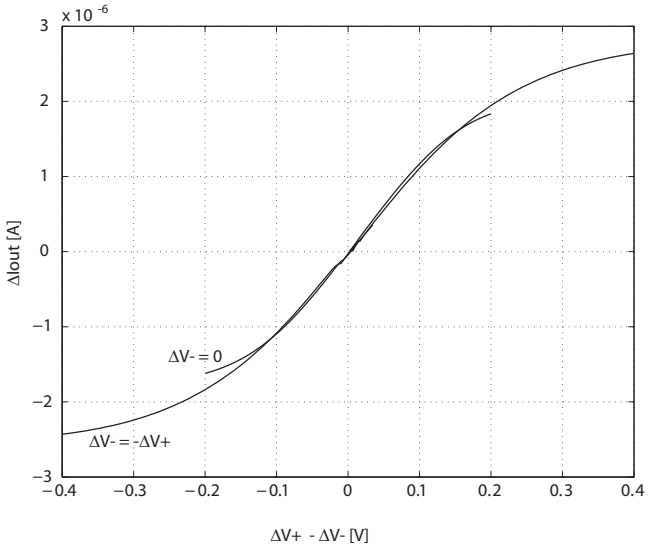

Fig. 6. *The output currents of the symmetric ULV transconductance amplifier. $V_{DD} = 300mV$. The output current is not determined by the dc level of the inputs.*

Simulated response of the symmetric transconductance amplifier is shown in Figure 6 where the clock signal frequency is $100MHz$. We applied an input signal to the positive input V_+, i.e $200MHz$ sine and a peak to peak amplitude equal to $200mV$ and a dc input to V_-.

The response of the ULV amplifer to a differential sine input and a varying supply voltage is shown in Figure 7. The supply voltage used in the simulation is a sine varying from $300mV$ to $500mV$. The supply voltage is used to recharge the evaluate transistors directly in the recharge mode and to power the amplifier in the evaluate mode. The aurozero level changes with the supply voltage and the response is not affected significantly by the the supply voltage or autozero level. The autozero level is always equal to $V_{DD}/2$. The differential sine input, V_+ - V_-, has an amplitude equal to $20mV$ and a dc voltage equal to $0V$. This is not natural in an autozero to half the V_{DD} system, but is used in this case to show that the dc level is not significant when the inputs are applied to capacitors.

A. ULV Voltage Integrator and Differentiator

By using the ULV amplifier in Figure 5 as a voltage follower we obtain the transfer function $\Delta V_{out} = \Delta V_+$. The circuit follows any change in the input signal when operated in the evaluation mode. By adding another amplifier with opposite clock signals and connect the inputs and outputs we obtain a continuous time voltage follower. The current running in the recharge mode is not significant to the overall performance of the circuit. In Figure 8 a ULV differentiator is shown.

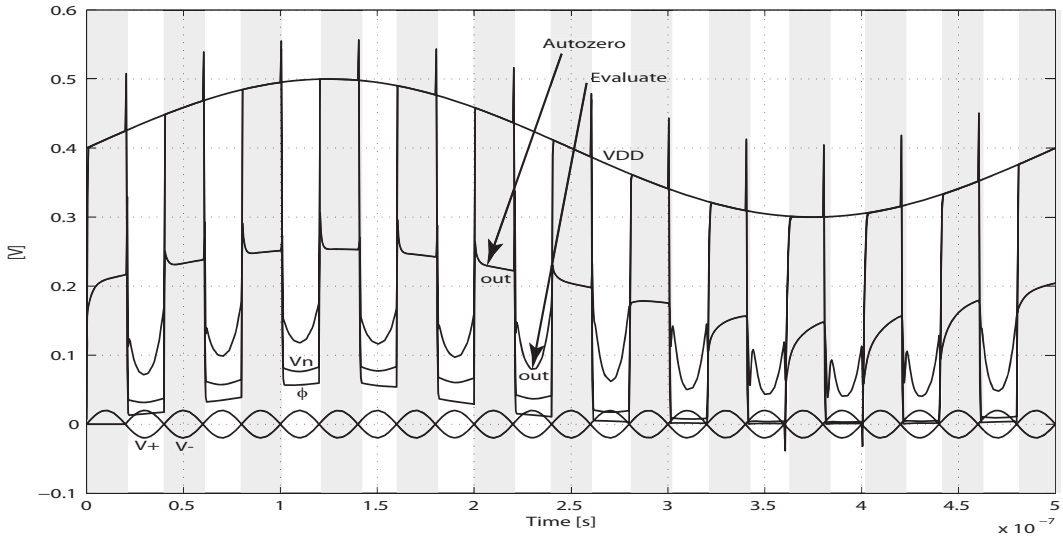

Fig. 7. *The response of the ULV amplifer to a differential sine input and a varying supply voltage.*

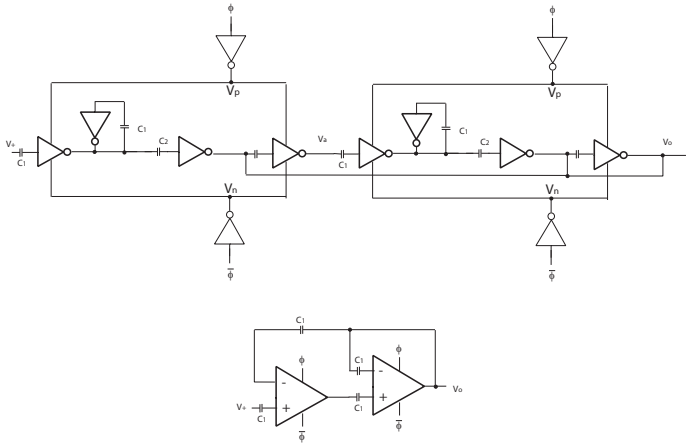

Fig. 8. *ULV differentiator.*

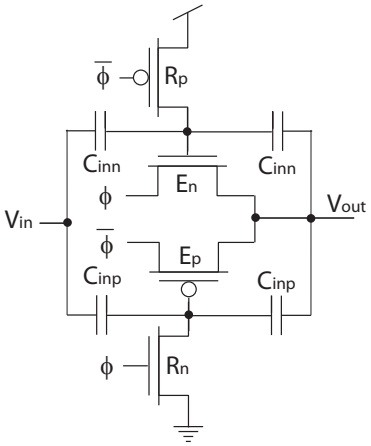

Fig. 9. *The analog inverter.*

B. Alternative symmetric transconductance amplifier

The single input analog inverter is shown in Fig. 9. The ideal response of the analog inverter may be expressed as $\Delta V_{out} = -\Delta V_{in}$. The gain is dependent on the transconductance to the output conductance ratio g_m/g_o of the circuit in evaluation mode. The gain is thus dependent on both the inherent transconductance and output conductance of the evaluate transistors and the capacitor ratio $C_{inn/p}/C_{fn/p}$.

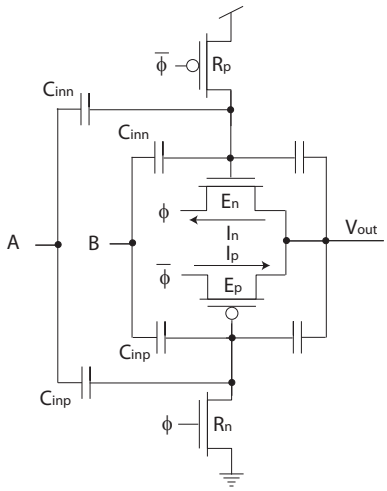

Fig. 10. *The double input analog inverter.*

The double input analog inverter is shown in Fig. 10. The circuit combines two inputs and provides an output defined by

$$\Delta V_{out} = G\left(\Delta A + \Delta B\right), \tag{2}$$

where G is the gain of the circuit. The gain is dependent on the transconductance and output conductance ratio of the evaluate transistors. Idealy the gain should be close to $G = -\frac{1}{2}$ in order to use the voltage headrom. If the inputs and outputs are precharged to $V_{DD}/2$ during the precharge phase, we secure that the output voltage is defined by equation (1). If we apply continuous input signals we may reduce the gain of the inverter, i.e. $|G| \leq \frac{1}{4}$ to be able to process input signals with a peak to peak amplitude equal to V_{DD}.

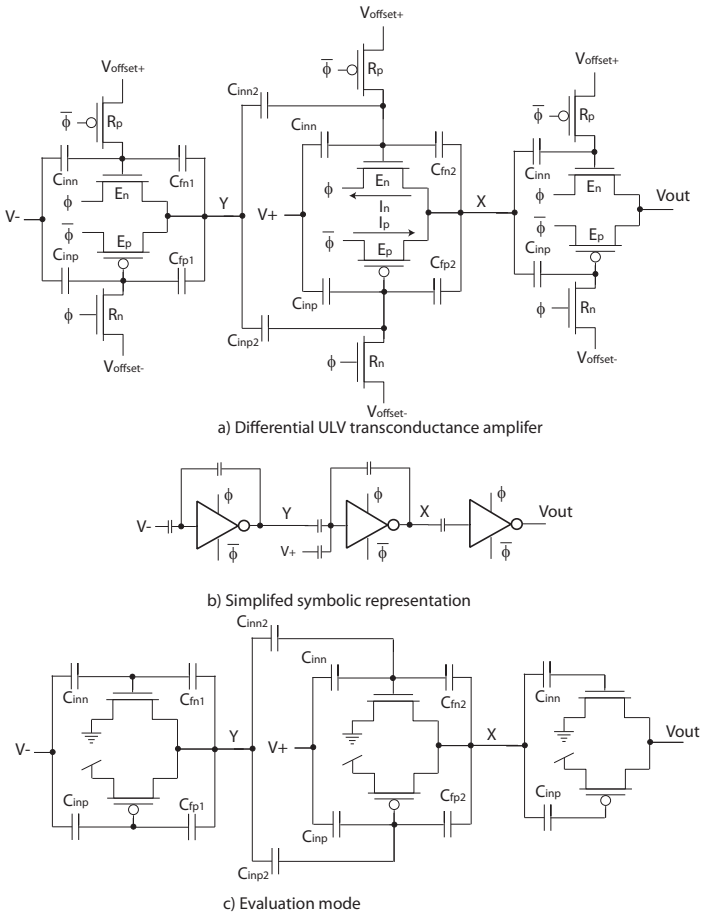

Fig. 11. *The ULV transconductance amplifier. a) transistor schematics, b) simplified representation and c) evaluation mode.*

The ULV gates presented perform an auto zeroing of each gate in each recharge phase. The output of each gate is determined by the mismatches inherent in each gate. Te dc level of the gate output may vary due to the inherent mismatches of the evaluate transistors feeding the output. The response of the gates are determined by voltage changes of gates providing the input signals and not the dc level of the inputs. There are no need for any dc-dc conversion due to the recharge phase forcing each gate output close to $V_{DD}/2$.

The analog inverter and a double input binary inverter can be used to design a simple ULV transconductance amplifier [**?**]. The pass-band ULV transconductance amplifier is shown in Fig. 11. The recharge transistors are connected to offset voltages which can be used to tune the frequency response of the amplifier. If we increase the offsets, i.e. $V_{offset+} > V_{DD}$ and $V_{offset-} < 0V$, the amplifier can process higher frequency input signals. The most practical offset voltages are V_{DD} and $gnd(0V)$. Other offset voltages can be be applied if external voltages or internally generated voltages are provided.

The response of the analog inverter and double input analog inverter to a sine signal with an amplitude equal to 75mV applied at input V_- and a DC signal(125mV) applied at input V_+ is shown in Fig. 12. Although the analog inverter providing the $\Delta Y = -\Delta V_-$ has a gain less than $|1|$ the signal can be combined with the input V_+ if the input capacitor connecting

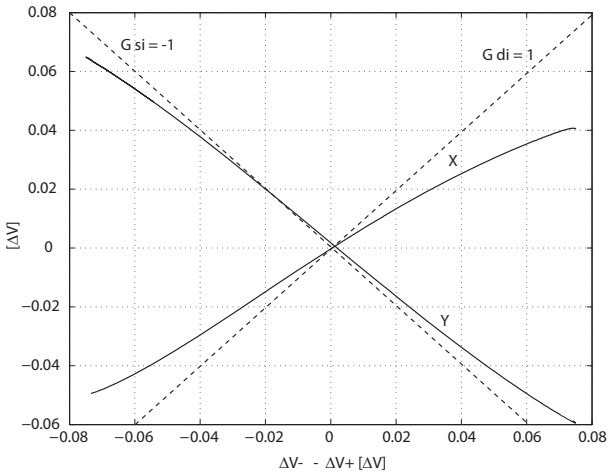

Fig. 12. *The response of the analog inverter and double input analog inverter to a input sine signal with a precharge level equal to $V_{DD}/2$ (125mV), i.e. $V_{DD} = 250mV$. G_{si} and G_{di} are the ideal gain of the single input and double input analog inverters respectively.*

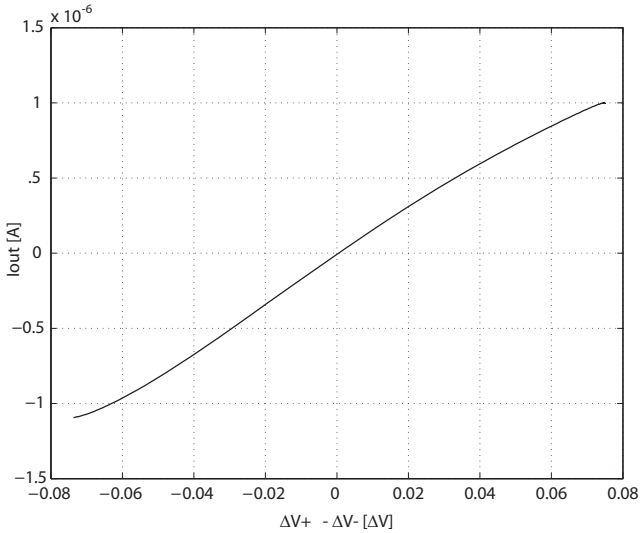

Fig. 13. *Output current of the ULV transconductance amplifier.*

Y to the double input analog inverter is increased compared to the capacitors connected to V_+. Furthermore the overall gain of the double input inverter is not critical. The gain seen from each input, i.e. V_- and V_+, should be equal in order to obtain a linear response of the amplifier. The feedback capacitors of the double input analog inverter is reduced to increase the overall gain of the amplifier, hence the gain is $|G| \approx 2/3$.

The output current of the ULV transconductance amplifier is shown in Fig. 13. The supply voltage is 250mV and the offset voltages are 350mV and -100mV.

As mentioned the frequency response is dependent on the offset voltages applied. The transconductance amplifier was simulated with a $sine$ input signal applied at the V_- terminal and a dc voltage applied at V_+ terminal. The supply voltage provided through the clock signals is equal to 250mV. The gain, $\Delta V_{out}/\left(\Delta V_+ - \Delta V_-\right)$ are shown. The data presented are obtained based on several transient simulations.

The frequency response of the ULV transconductance am-

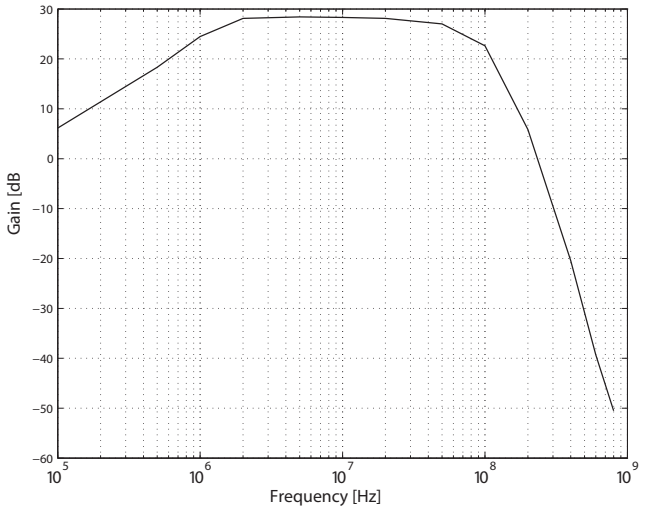

Fig. 14. *The frequency response of the ULV transconductance amplifier with offset voltages equal to 250mV and 0V.*

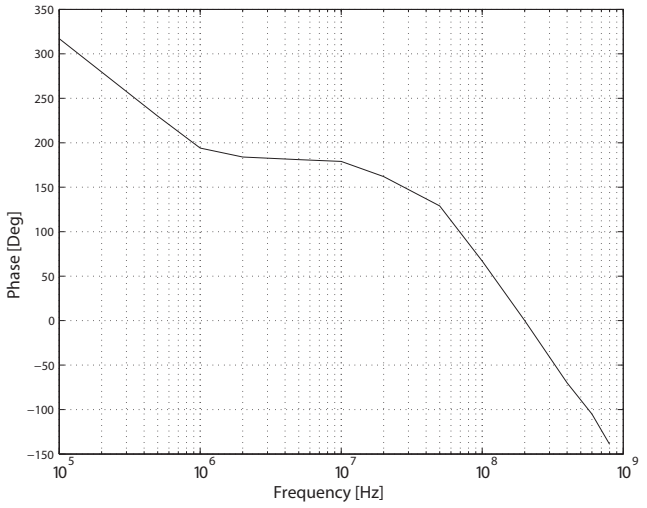

Fig. 15. *The phase of the ULV transconductance amplifier with offset voltages equal to 250mV and 0V.*

plifier with offset voltages equal to 250mV and 0V is shown in Fig. 14 and the phase is shown in Fig. 15. The passband is 1.8MHz to $60MHz$ and the gain is close to 30dB.

The frequency response of the ULV transconductance amplifier with offset voltages equal to 350mV and -100mV is shown in Fig. 16. The gain has been reduced compared to the frequency response shown in Fig. 14 due to a higher current level and thus reduced relative transconductance. The gain is approximately 10dB and the cut off frequency is 300MHz, i.e the passband is 18MHz to 300MHz.

IV. Conclusion

The amplifier allows rail to rail signals an no need for dc-dc conversion is required. The ULV amplifier is not directly connected to the power supply and the response of the amplifier is not significantly affected by varying supply voltage. The transconductance amplifier may operate at a supply voltage equal to the threshold voltage of the nMOS transistor in a $90nm$ CMOS process.

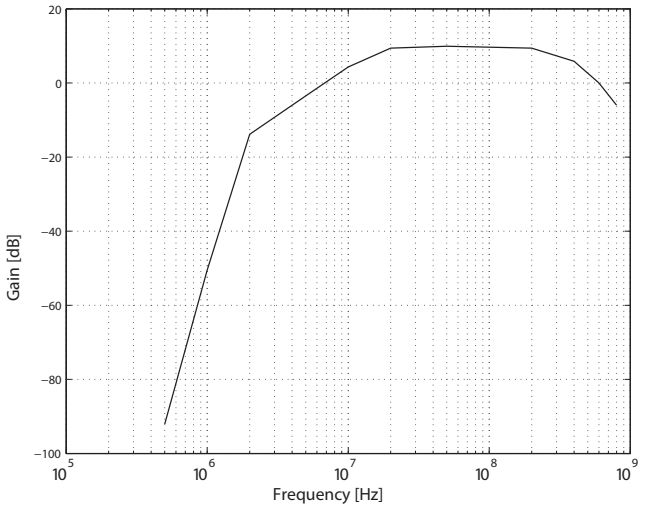

Fig. 16. *The frequency response of the ULV transconductance amplifier with offset voltages equal to 350mV and -100mV.*

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