Static Differential Ultra Low-Voltage Domino CMOS logic for High Speed Applications

Yngvar Berg and Omid Mirmotahari

***Abstract*— In this paper we present a novel static differential ultra low-voltage (ULV) CMOS logic style for High-Speed applications . The proposed logic style is aimed for high speed serial adders in ultra low-voltage applications. The differential ultra low-voltage inverter presented have less than 10% of the delay than standard CMOS inverters for supply voltages less than $500mV$. The simulated data presented is obtained using $Hspice$ simulator and applying a $90nm$ $TSMC$ CMOS process.**

***Index Terms*— CMOS, Low-Voltage, Domino logic, Differential logic, High-Speed, Digital.**

I. Introduction

Low voltage digital CMOS becomes more and more interesting, due to the general advances in process technology and due to new low power applications. In most digital applications the use of arithmetic operations is extensive. The focus on low-voltage digital systems is increasing in general due to technology advances and especially beneficial for low power design. Furthermore, low voltage design may offer a benefit in terms of flexibility in power sources, i.e. different battery options.

Low voltage does not necessarily imply low power; the power consumed by a gate is proportional to the active current driving the output of the gate. Hence, delay and power consumption are both dependent on the current and the energy or power delay product (PDP) is not significantly dependent on the current. The energy required to toggle a bit is more dependent on the load and configuration of the gate. Energy delay product (EDP) is more dependent on speed than on power and will be improved by increasing the current for a specific supply voltage. The optimal supply voltage for CMOS logic in terms of EDP is close to the threshold voltage of the nMOS transistor V_{tn} for a specific process, assuming that the threshold voltage of the pMOS transistor V_{tp} is approximately equal to $-V_{tn}$ [1]. Several approaches to high speed and low voltage digital CMOS circuits have been presented [2].

Typical arithmetic operation, for example a full adder, may be implemented in numerous ways using different CMOS logic styles. In addition the option of using parallel or serial adders makes the choice even more challenging. In a typical adder the critical delay is linked to the carry propagation. By using complex carry look ahead techniques or applying parallel structures the delay can be reduced compared to a simple serial adder. The cost comes in increased, complexity, power consumption and chip area.

Floating-Gate (FG) logic implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than than provided by the supply voltage headroom [3]. There are several approaches to FG CMOS logic [4], [5]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits [6]. Floating-Gates have been used for analog circuits as well[7]. Different ULV logic styles are presented in section 2 and simulation results are presented in section 3.

II. Ultra-Low-Voltage Semi-Floating-Gate Logic

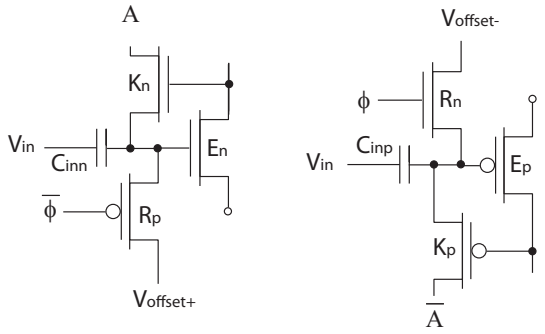

Fig. 1. Static clocked semi-floating-gate (CSFG) transistors.

The ULV logic styles presented in this paper are related to the ULV domino logic style presented in [8], [9], [10]. The main purpose of the ULV logic style is to increase the current level for low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra loads represented by the floating capacitors are less than extra the load given by increased transistor widths. The capacitive inputs lower the delay through increased transconductance while increased transistor widths only reduce parasitic delay. The ULV logic styles may be used in critical sub circuits where high speed and low supply voltage is required. The ULV logic styles may be used together with more conventional CMOS logic. A ULV high speed serial carry chain [11] has been presented using a simple dynamic ULV logic [12]. The technique using a semi floating-gate to increase the current

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level have been applied to low voltage Flip-Flops [13]. In this paper we exploit an NP domino ULV static differential logic style.

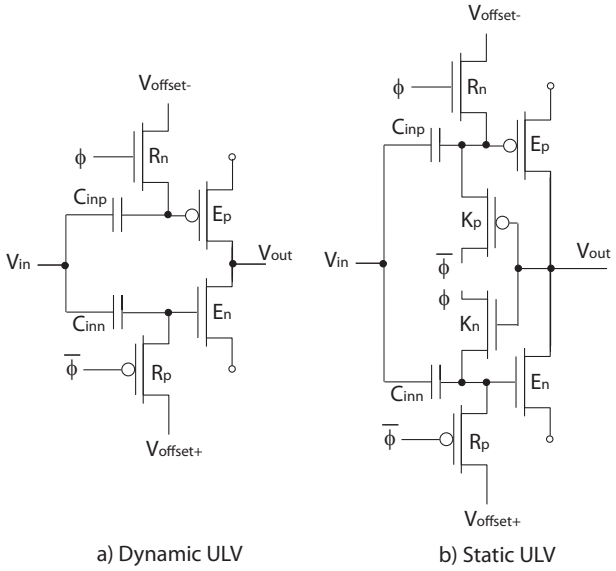

Fig. 2. a) simple ULV inverter and b) static ULV domino logic inverter.

The simple dynamic ULV inverter is shown in Fig. 2 a) and the static ULV inverter is shown in Fig. 2 b). There are two ways to configure these inverters:

1) Apply clock signals to power the inverter, i.e. connect transistor E_n to ϕ and E_p to $\overline{\phi}$ and precharge the output to $V_{DD}/2$ (=1/2) when $\phi = 1$. This is called precharge or recharge mode due to the recharge of the gates through the recharge transistor R_n and R_p. The gate will be forced to 0 or 1 in the evaluation mode depending on the input transition.
2) Apply a clock signal to power the inverter, i.e. either ϕ to E_n and V_{DD} to E_p, or $\overline{\phi}$ to E_p and GND to E_n and precharge to 1 or 0 respectively. The gate resembles NP domino logic. In order to hold the precharged value until an input transition arrives the E transistor connected to a supply voltage is made stronger than the other E transistor.

In Fig. 2 b) keeper transistors K_p and K_n are included to reduce static power and increase noise margin. The keeper transistor will reset the non-active transistor and hence reducing the static current which matches the OFF current in a complementary CMOS inverter. A simple model for the noise margin is given by $NM = I_{on}/I_{off}$. Thus, by adding keepers we may increase the noise margin for the static ULV logic compared to complementary CMOS.

A severe problem when using the static ULV logic, shown in Fig. 2, in carry chains is that the output is floating until an input transition occurs. If the output for some reason, noise or mismatch, starts an erroneous transition the gate will eventually be locked in a false state and will not respond to a slow input transition. We may overcome this problem by applying a differential scheme where two gates enable each other at the right time.

A. Static Differential Ultra Low-Voltage Logic

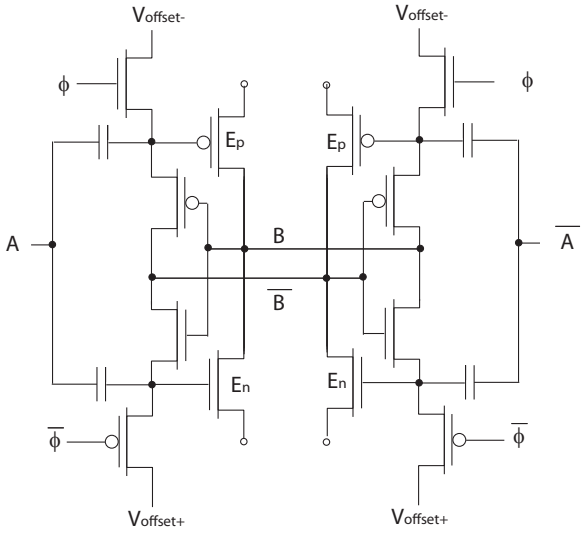

Fig. 3. Static differential ULV NP domino (SDNPU) inverter.

The static differential NP domino ULV logic is shown in Fig. 3. If we apply ϕ to the E_n transistors and V_{DD} to the E_p transistors we precharge both outputs to logic 1 in the recharge mode, hence $B = \overline{B}$. The pMOS keepers will be turned off and the nMOS keepers will be turned on holding the initial recharge value of the nMOS transistor. The only way to turn the keepers ON is to pull one of the outputs towards 0. Furthermore, the SDNPU inverter is suitable for large logic depths. The good noise margin secures stable signal values with insignificant static power consumption.

The different ULV logic styles are defined by the applied terminal inputs as shown in Table I. The ON and OFF currents of a complementary CMOS inverter is given by the effective gate source voltages V_{DD} and $0V$ respectively. Assuming $\frac{Cin}{CT} = 0.5$ where C_T is the total capacitance seen by a floating gate, we may estimate the delay, dynamic and static power and noise margins of the different ULV logic styles relative to a complementary CMOS inverter.

B. Domino and Latch Configurations

The different configurations of static differential ULV logic inverters are shown in Fig. 4. By inverting the clock signals we obtain a latch configuration. The latched signal is available through a gate leaving the evaluation mode and entering the recharge mode. The edge created in the precharge process forces the next gate to respond to the edge and the output will be equal to the latched state. However, the delay of the first gate responding to a latched value will be large compared to the delay further down the chain. The reason for this increased delay is the time required to precharge.

III. Simulation Results

The data presented is based on a 90nm TSMC CMOS process and the load applied is an identical gate for each

ΔV	E_p	E_n	K_p	K_n	$V_{gs}\ I_{ON}$	$V_{gs}\ I_{OFF}$	NM^*	Style	Comment
$\pm\frac{V_{DD}}{2}$	$\overline{\phi}$	ϕ	–	–	$\frac{5V_{DD}}{4}$	$\frac{3V_{DD}}{4}$	$\frac{V_{DD}}{2}$	DU	Dynamic
$\pm\frac{V_{DD}}{2}$	$\overline{\phi}$	ϕ	$\overline{B}$	$\overline{B}$	$\frac{5V_{DD}}{4}$	0	$\frac{5V_{DD}}{4}$	SDU	Static differential
V_{DD}	$\overline{\phi}$	GND	–	–	$\frac{3V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	DNU	Dynamic prech. 0
V_{DD}	$\overline{\phi}$	GND	$\overline{B}$	$\overline{B}$	$\frac{3V_{DD}}{2}$	0	$\frac{3V_{DD}}{2}$	SDNU	Static differential prech. 0
$-V_{DD}$	V_{DD}	ϕ	–	–	$3\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	DPU	Dynamic prech. 1
$-V_{DD}$	V_{DD}	ϕ	$\overline{B}$	$\overline{B}$	$\frac{3V_{DD}}{2}$	0	$\frac{3V_{DD}}{2}$	SDPU	Static differential prech. 1

TABLE I

ULV LOGIC STYLES. ΔV IS THE OUTPUT VOLTAGE SWING. THE SIMPLE MODEL FOR THE NOISE MARGIN NM^* IS GIVEN BY THE RATIO OF THE ON CURRENT AND THE OFF CURRENT. THE CAPACITIVE DIVISION FACTOR, $\frac{Cin}{CT}$ WHERE C_T IS THE TOTAL CAPACITANCE SEEN BY A FLOATING GATE, IS ASSUMED TO BE 0.5.

Style	Comment	200mV	250mV	300mV	350mV	400mV	450mV	500mV
CLK	Delay (ns)	12.2	3.75	1.28	0.47	0.215	0.119	0.078
	f_{clk} (MHz)	10.2	33.3	98	266	581	1050	1602
CMOS	Delay (ns)	47,5	14.85	4.98	1.865	0.78	0.37	0.20
NP	Delay (ns)	67,5	21.95	7.45	2.79	1.18	1.58	0.305
DU	Delay (ns)	4.83	1.295	0.385	0.175	0.059	0.03	0.0255
	Relative delay (%)	10.2	8.7	7.7	9.4	7.6	8.1	12.8
	Delay latch + 8 gates (ns)	82.12	22.69	7.01	2.64	1.003	0.493	0.30
	Level ($\%V_{DD}$)	93.0	96.6	97.4	97.2	99.3	94.2	92.6
	f_{max} (MHz) (LD=10)	5.45	19,78	64.27	167.2	446	904	1425
	Max logic depth (LD)	3	4	5	5	7	9	10
SDU	Delay (ns)	12.46	3.72	1.27	0.49	0.165	0.092	0.083
	Relative delay (%)	26.2	25.1	25.5	26.3	21.2	24.7	41.5
	Delay latch + 8 gates (ns)	172	46.27	14.65	5.63	2.207	1.199	0.846
	Level ($\%V_{DD}$)	98.5	99.1	99.3	99.5	99.8	99.4	99.7
	f_{max} (MHz) (LD=10)	2.5	9.3	25.5	29.2	74.9	197	362
	Max logic depth (LD)	0	1	2	2	2	2	3
DNPU	Delay (ns)	0.96	0.325	0.125	0.059	0.040	0.034	0.032
	Relative delay (%)	2.0	2.2	2.5	3.1	5.1	9.1	16
	Delay latch + 8 gates (ns)	27.52	7.89	2.65	1.141	0.669	0.460	0.470
	Level ($\%V_{DD}$)	99.2	96.0	95.0	92.6	86.7	74.6	
	f_{min} (MHz) (LD=10)	1.6	1.0	3.7	8.3	45.5	192	
	f_{max} (MHz) (LD=10)	17	59	172	397	667	949	936
	Max logic depth (LD)	32	32	30	23	15	10	5
SDNPU	Delay (ns)	3.125	0.885	0.270	0.170	0.056	0.040	0.032
	Relative delay (%)	6.6	6.0	5.4	9.1	7.2	10.7	16
	Delay latch + 8 gates (ns)	57.31	15.23	4.8	1.779	0.92	0.541	0.404
	Level ($\%V_{DD}$)	99.7	99.7	99.8	99.8	100	99.8	99.7
	f_{max} (MHz) (LD=10)	7.9	29.4	95	226	485	806	1068
	Max logic depth (LD)	7	9	11	10	9	8	7

TABLE II

Timing details if the ULV logic styles compared to complementary CMOS and NP domino logic.

logic style. The ULV inverters are first latched and then passed through a chain of 10 inverters. The simulated data is compared to the delay of a chain of complementary CMOS inverters where the total delay through a specific number of inverters corresponds to the operating frequency of the ULV inverter chain. Average values per gate are presented in this section.

The average energy per gate of the static differential NP domino ULV (SDNPU) inverter relative to a complementary inverter is shown in Fig. 5. The dynamic or switching energy of the SDNPU is close to the switching energy of a complementary CMOS inverter operating at the same supply voltage. During the time in evaluation mode before a gate toggles the gate waits in a biased state. The energy required to hold the precharged state relative to the switching energy of a complementary inverter switching is shown in Fig. 5 and labeled $Wait$. The relative static power and recharge power compared to static energy of a complementary is also shown for different supply voltages. As expected the power required to hold the recharged/precharged value exceeds the power required for a complementary inverter to hold a stable state.

The average relative delay per gate of the ULV logic inverter chain is shown in Fig. 6. In general the simple dynamic versions are faster than their static versions due to less loads. The DNPU and SDNPU logic style is very fast due to the large current level given by the effective gate-source voltage equal to $3V_{DD}/2$. Compared to complementary CMOS the delay of the differential ULV inverters are less than 10% of a complementary CMOS inverter.

The average relative energy of the ULV logic inverters

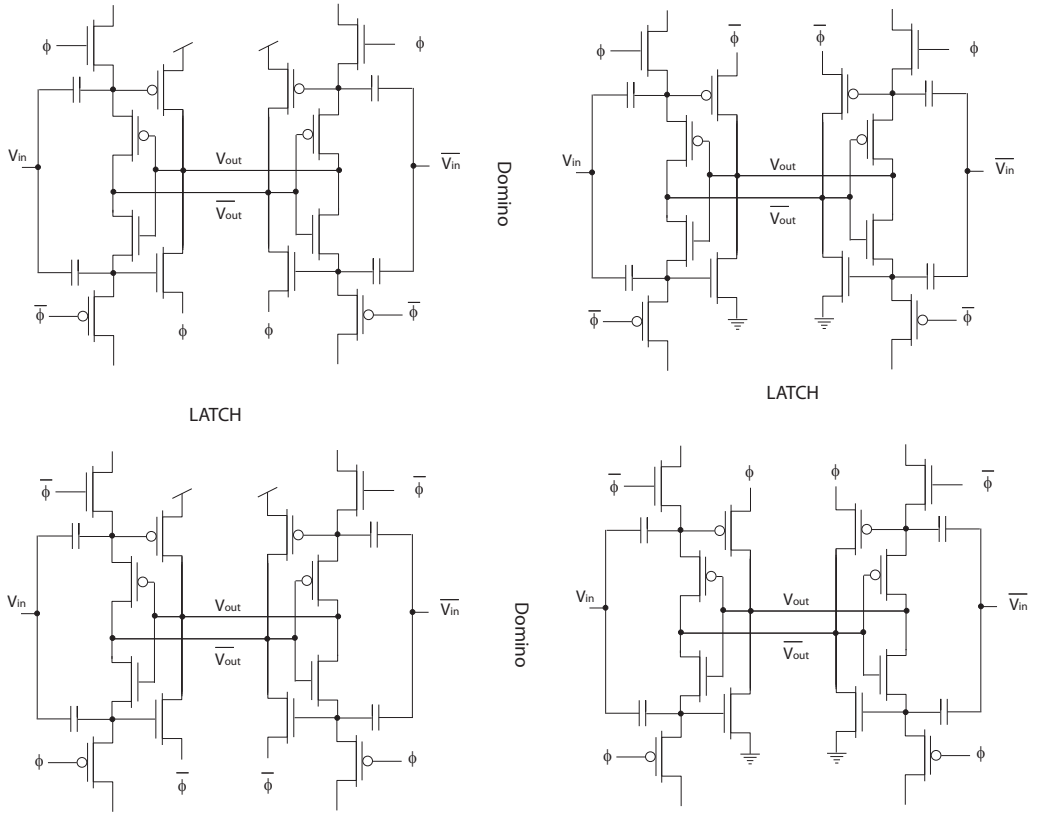

Fig. 4. Different configurations of static differential ULV logic inverters.

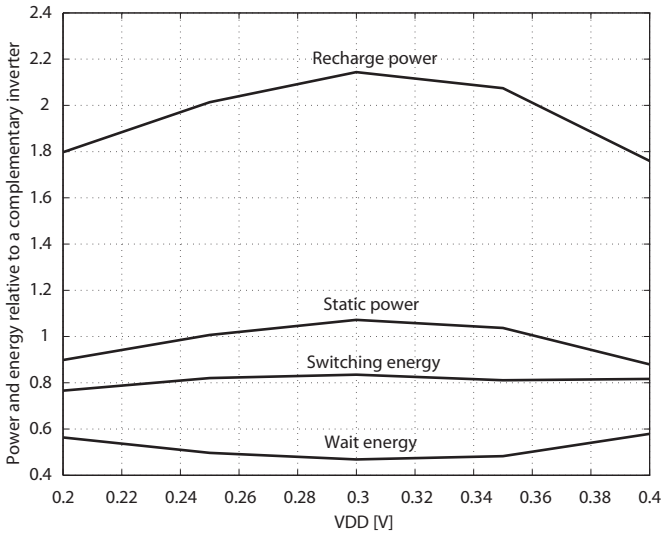

Fig. 5. Average relative energy and static power consumption per gate for different supply voltages.

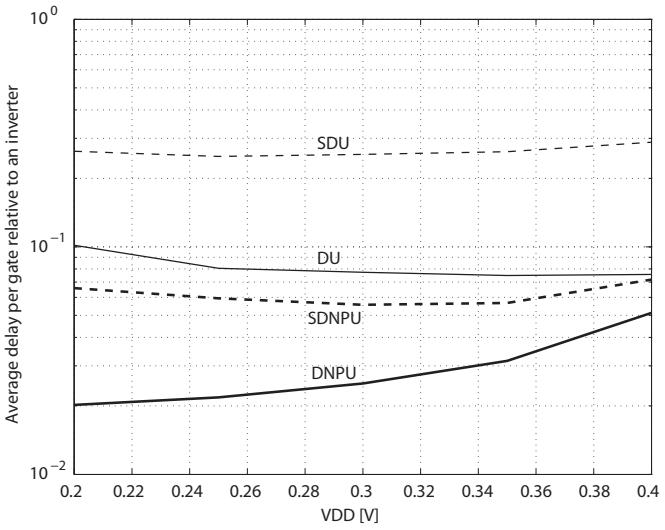

Fig. 6. Average relative delay per gate of the ULV logic inverter chain.

for different supply voltages is shown in Fig. 7. The power-delay-product (PDP) of the differential gates will be increased compared to the non-differential gates due to more complex circuitry and to the local feedback to the floating-gates. The SDU logic style has an average PDP larger than complementary CMOS.

The average relative energy delay product (EDP) of the ULV logic inverters is shown in Fig. 8. The dynamic ULV gates are characterized by low EDP compared to static ULV versions. Furthermore, the differential logic styles are preferable due to low EDP. The EDP of the static differential ULV inverter is only 4% of the EDP of a complementary inverter.

The noise margin for the ULV logic styles relative to a complementary inverter is shown in Fig. 9. As expected the noise margins for the static ULV inverters are improved compared to complementary CMOS for low supply voltages

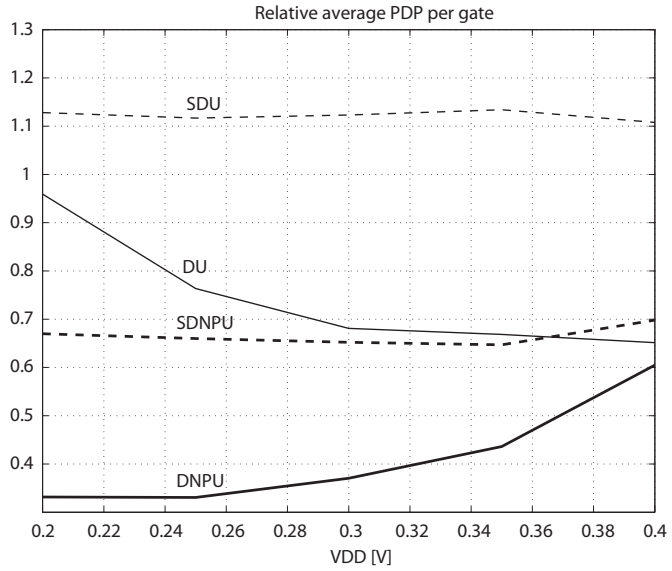

Fig. 7. Average relative energy of the ULV logic inverters.

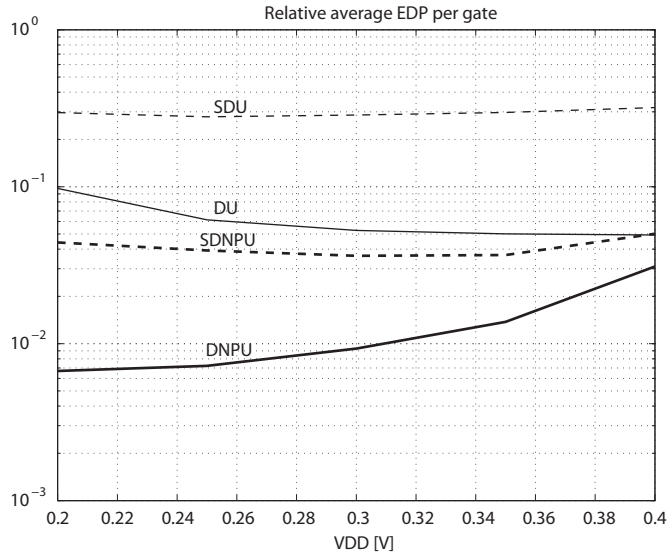

Fig. 8. Average relative energy delay product (EDP) of the ULV logic inverters.

while the noise margins for the dynamic gates are worse than for complementary CMOS. The relative noise margin for the dynamic ULV gates will be reduced when the supply voltage is increased due to the large OFF current of the dynamic ULV gates.

The power consumed by the clock drivers are not included and must be taken into consideration for each specific application. Whenever latching is required the clock signals must be provided. The ULV logic styles can be compared to precharge logic in terms of clock load. The latching is however less clock demanding than conventional CMOS latches and flip-flops.

The timing details of the ULV logic styles, complementary CMOS and NP domino logic are shown in TABLE II for supply voltages from $200mV$ to $500mV$. For each logic style the average delay is compared to standard CMOS and NP domino logic. The delay of a latch and 8 subsequent gates is

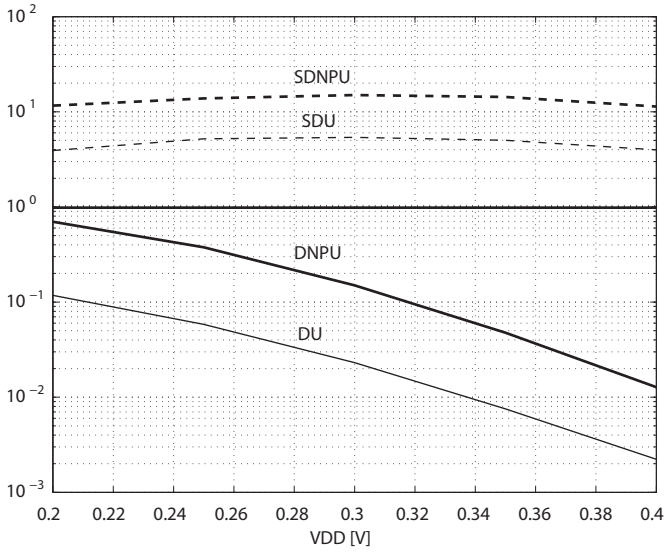

Fig. 9. The noise margin for the ULV logic styles relative to a complementary inverter.

shown together with the noise margin or ouput voltage level, maximum frequency given a logical depth (LD) of 10, and the maximum logical depth given the clock frequency (f_{clk}). Furthermore, the minimum clock frequency of the dynamic DNPU style is shown.

The timing details show that the different ULV logic styles can be used to implement high speed ultra low-voltage circuits. The DU logic style is approximately 10 times faster than standard CMOS while the SDU logic style is comparable to standard CMOS. However, the output voltage level is very close to V_{DD} for the SDU wheras the output level of the DU logic style is less close to V_{DD}. The noise margin of the SDU is far better than for the DU logic. The differential NP domino ULV logic styles, DNPU and SDNPU, are very fast compared to standard CMOS and NP domino logic. The delay of the DNPU inverter for a supply voltage equal to $200mV$ is only 2% of the delay for a standard inverter. However, the noise margin is significantly reduced and the DNPU logic style will not work properly for supply voltage above $450mV$. The static differential NP ULV logic style SDNPU is both fast and robust as shown in TABLE II.

IV. Conclusion

We have presented different ultra low-voltage (ULV) CMOS binary logic styles. The static differential ULV logic style can be used for low-voltage high-speed digital systems, and may be used together with standard low-voltage CMOS. The different ULV logic styles are fast compared to both standard CMOS and NP doimno logic. The energy delay product of the static differential inverter is less than 10% of complementary inverters as shown in Fig. 8.

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