Filter implementation for CMOS adaptive sampling Delta Modulators

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Abstract — We illustrate the idea of the building delta modulator/demodulator with the help of the non-uniform sampling method. Each of element, both analog and digital, that is used for this realization can be put together on one chip, making up a piece of the System on Chip circuit or the ASIC chip dedicated to special purpose, such as: measuring, communication, control systems, data compression, data encryption wireless telecommunication. The Adaptive Non-uniform Sampling Delta Modulators (ANS-DM) modulation algorithm implementations, and the codec architecture are described in the paper also.

We present a comparative study of integrated CMOS continuous time (CT) analog filters dedicated for speech codecs with adaptive non-uniform sampling. Five CMOS implementations of this block have been studied, four of them fabricated in 0.35 μm CMOS technology. The system considerations and simulation results are shown.

Keywords — adaptive delta modulation, CMOS circuits, switched-capacitor filters, continuous time filters, anti-aliasing filters, non-uniform sampling, speech codecs.

I. INTRODUCTION

THE investigation aimed at the improvement of analog to digital conversion efficiency prove that not all potential possibilities of delta modulation analog signal processing have been fully utilized, so far [1]. The concept of using adaptive sampling to reduce the data rate of source coding is very promising theme, however studied only fragmentarily [2].

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The long-term research works [1, 3, 4] allow to affirm, that reaching high accuracy and large noise immunity in wide dynamic range, with use of the uniform sampling ADM converters, is not possible. Therefore we propose use of the 2 – parameters, 1-bit PCM differential modulation, which in fact depends on application of adaptation of both the step size and sampling interval. The results of simulating works proved that for nonstationary sources, the adaptive sampling delta converters expose higher coding efficiency than the former proposals, based on uniform sampling methods.

Classification and evaluation of the ADM converters solutions presented in the works [4, 5], including conceptual studies, enabled construction of the adaptive sampling converters (NS-DM and ANS- DM) prototype circuits. The studies of the solutions proved that, at present, fully efficient hardware implementation of adaptive sampling delta converters conception on the base of microprocessor standard chips, is possible.

The work was aimed at elaboration of analyze methods and performance evaluation of the filters for delta systems with step size and sampling rate adaptation. It comprised the studies of mathematical description, computer simulations, and design methodology, as well as proposal of electronic circuits implementation. Within analytical part, the method of description of the performances of the filters for adaptive sampling delta converters has been worked out.

The method of design of the filters architecture was proposed.

In simulating investigations, performance of the filters were analyzed. The unique approach to this investigations enabled comprehensive comparison of former and new solutions.

Each practical design must be done in specific technology, so initially our choice was an 2P4M 0.35μm CMOS technology from austriamicrosystems (AMS), and all the presented simulation/measurements are done for this specific silicon foundry. However the circuit solutions are transferable into more advanced technology node (e.g. 180nm CMOS from United Microelectronics Corporation) with improved elements – especially capacitors which have significantly lower parasitics. NMOS and PMOS transistors for AMS 0.35 technology have threshold voltages varying between $-0.68 \div -0.72$ Volt and $0.46 \div 0.59$ Volt, respectively. In the framework of our project we investigated 5 different filters, 4 of them were manufactured as a part of four test chips.

II. PRINCIPLE OF THE ANS-DM MODULATIONS

A. Functional diagram and algorithm of the ANS-DM modulations

The ANS-DM is a modulation, where both coder parameter's: the step size and the sampling instant are adopted. Changes of the input signal level cause adequate a sampling frequency and a step size adaptation (Fig.1). This

modulation has slightly better coding quality so *SNR* is closer to its maximal value then others delta modulations (LDM, NS-DM) were.

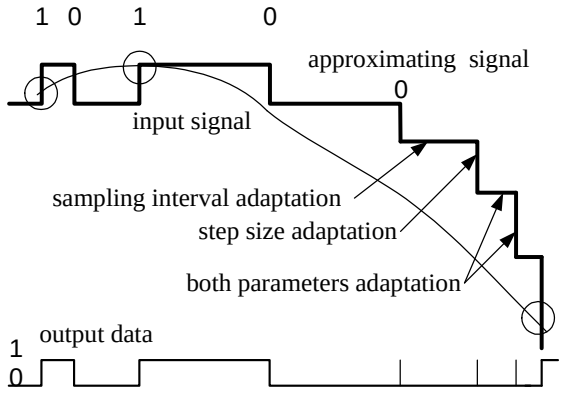


Fig. 1. Timings of the ANS-DM modulation.

The ANS-DM scheme has been proposed and studied in [2, 5]. The block diagram of its idea is presented in Fig.2. ANS-DM base on the Modified Interval Function (MIF) and the Modified Step-size Function (MSF). The MIF function modifies the sampling interval while the MSF modifies the step size according to the time-varying slope characteristics of the input process. In this way a staircase waveforms fit to the source signal better by ANS-DM than others delta modulations (LDM, NS-DM).

For the input signal $x(t)$ the predicted signal $s(t_i)$ is given by expression (1):

$$s(t_i) = s(t_0) + \sum_{n=1}^{i-1} k_i d_i \qquad (1)$$

$$where: \quad d_i = \operatorname{sgn}[x(t_i) - s(t_i)]$$

and k_i – i-th step size.

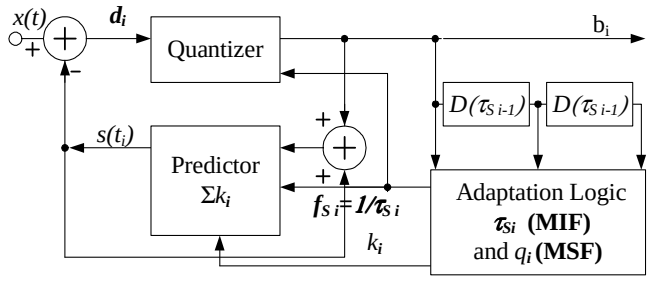
The output code stream is:

$$b_i = \begin{cases} 1 & for \quad d_i = 1 \\ 0 & for \quad d_i = -1 \end{cases} \qquad (2)$$

Let τ_s be the sampling instant and $s(t_i)$ - the approximation signal $x(t)$ at t_i. The sampling instant $\tau_s = t_{i+1} - t_i$ vary according to the characteristics of $x(t)$ thus the next sampling time t_{i+1} is expressed as:

$$t_{i+1} = t_i + \tau_s \qquad (3)$$

a)



b)

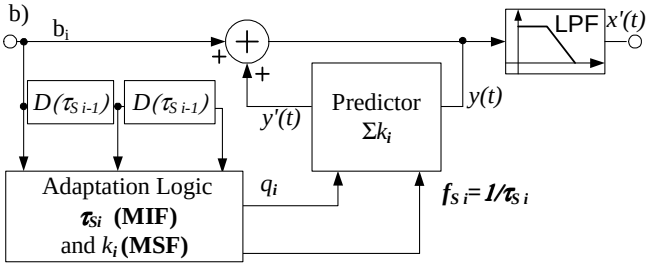


Fig. 2. Block diagram of ANS-DM modulator: a) modulator, b) demodulator.

The sampling instant τ_s is changed according to following algorithm:

$$\tau_s = \begin{cases} P \cdot \tau_{s-1} & \text{for MIF} > 1 \\ Q \cdot \tau_{s-1} & \text{for MIF} < 1 \\ \tau_0 \text{ for MIF} = 1 \end{cases} \qquad (4)$$

where: MIF for ANS-DM is described by Table 1; *P*, *Q* are the constant factors of sampling instant modification and their values are: $Q<1<P$. In this case τ_s is placed between the upper bound τ_{max} and the lowest one τ_{min}. The τ_0 is start sampling instant and its value decides about the average output bit rate [5, 6].

Table 1. MIF and MSF functions

b_i	b_{i-1}	b_{i-2}	S_i	T_i	S_{i-1}	T_{i-1}	MSF	MIF
0	0	0	0	1	0	0	1	<1
			1	0	0	1	>1	1
			1	1	1	0	>1	<1
			1	1	1	1	>1	<1
0	0	1	0	0	H	H	1	1
0	1	0	0	1	H	H	1	>1
0	1	1	0	0	H	H	1	1
1	0	0	0	0	H	H	1	1
1	0	1	0	1	H	H	1	>1
1	1	0	0	0	H	H	1	1
1	1	1	0	1	0	0	1	<1
			1	0	0	1	>1	1
			1	1	1	0	>1	<1
			1	1	1	1	>1	<1

A value of step size k_i is modified according formula:

$$k_i = \begin{cases} R \cdot k_{i-1} & \text{for MSF} > 1 \\ k_i \text{ for MSF} = 1 \end{cases} \qquad (5)$$

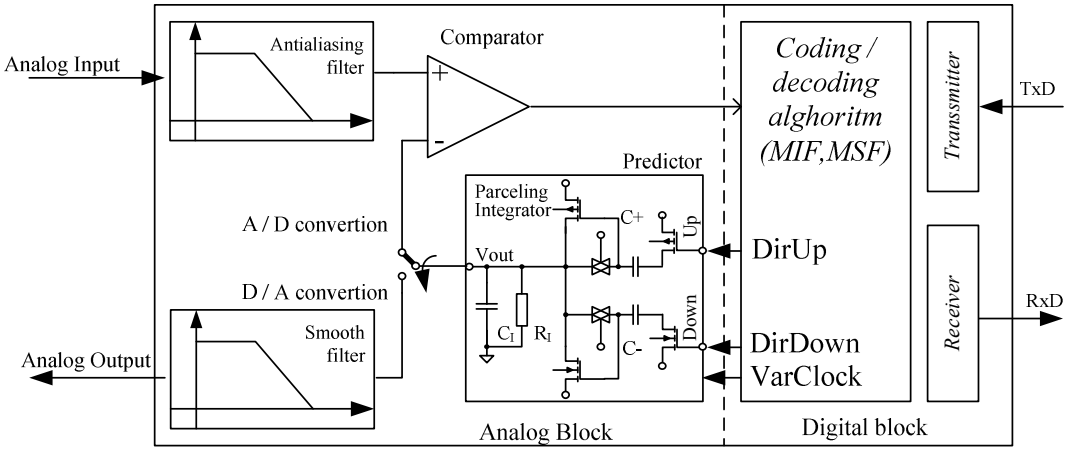


Fig. 4. Block diagram of the ANS-DM modulator/demodulator architecture with the modified R.Laane- B.T. Murphy parceling integrator [7]

where MSF is described by Table 1; *R* is the constant factor of step size modification and *R*>1.

Formulas (4, 5) represents 3-bit Zhu adaptation algorithm for ANS-DM modulation [6]. The symbols: "<1", ">1", "1" mean: decreasing, increasing, and coming back to start value of coder parameters. S_i, T_i – flags.

The ANS-DM output bit stream carries the information of not only the changing up or down of the input signal but also of the sampling instants and the step size value of the modulator.

B. Non-uniform sampling CODEC architecture

The ANS-DM codec architecture, shown on fig.3, is the result of the many research and simulation experiments. This solution consists of the five major elements: analog antialiasing input filter, comparator, adaptation logic block with the sampling frequencies/instant generator, d/a converter (parceling integrator) and output smooth filter (Fig.3).

Codec uses Zhu algorithm [6], that is hardware implemented as adaptation logic block. Both encoding and decoding process are the same, therefore, block contains identical components: the coincidence shift register, programmable clock divider and MIF (Fig. 4). All mentioned parts, establish the time duration of the sampling instant. The next sample is triggered by the programmable clock, but to eliminate computational complexity of frequency setting, all necessary parameters are calculated at the beginning of conversion and then store as a divider value in the Frequency Table.

Predictor circuit (Fig.4), which reconstructs the input signal, is known as a charge parceling integration [7, 8]. This integration technique charges the capacitor C_I only by a quantum of charge. A controlled amount of the charge is current independent and it causes that a constant value of voltage is added to or subtracted from the integrating capacitor C_I. Since the charge transfer is completely within a few nanoseconds the widths of the pulses from output gates do not affect the charge process consequently. The use of the charge parceling integration technique avoids step size variations due to timing fluctuations in the stair case appearance of the predicted signal [7, 8].

The analog input filter for the ADM encoder realization should be similar to classical PCM AAF (anti-aliasing filters) [9].

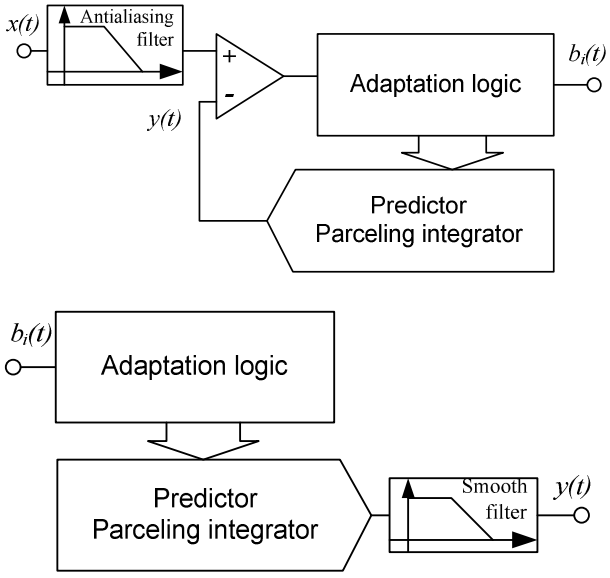


Fig.3. Simplified ANS-DM coder/decoder block diagram.

III. FILTER SPECIFICATIONS

In PCM codecs usually switched-capacitor (SC) filters are used for anti-aliasing purposes. SC filters have very good performance and fulfill sharp PCM requirements – passband ripple 0.125dB, idle noise < 6dBrnc0, group delay less than 110us and –32dB/1600Hz roll-off. The main drawback of this class however is higher noise level, which results with worsening signal-to-noise ratio, as well as higher (compared with continuous time (CT) filters class) power consumption [1, 10]. Usually SC filter needs a clock signal with frequency 100 times larger than cut-off frequency (3.4 kHz for most speech applications). However in the case of adaptive non-uniform sampling delta modulators constant

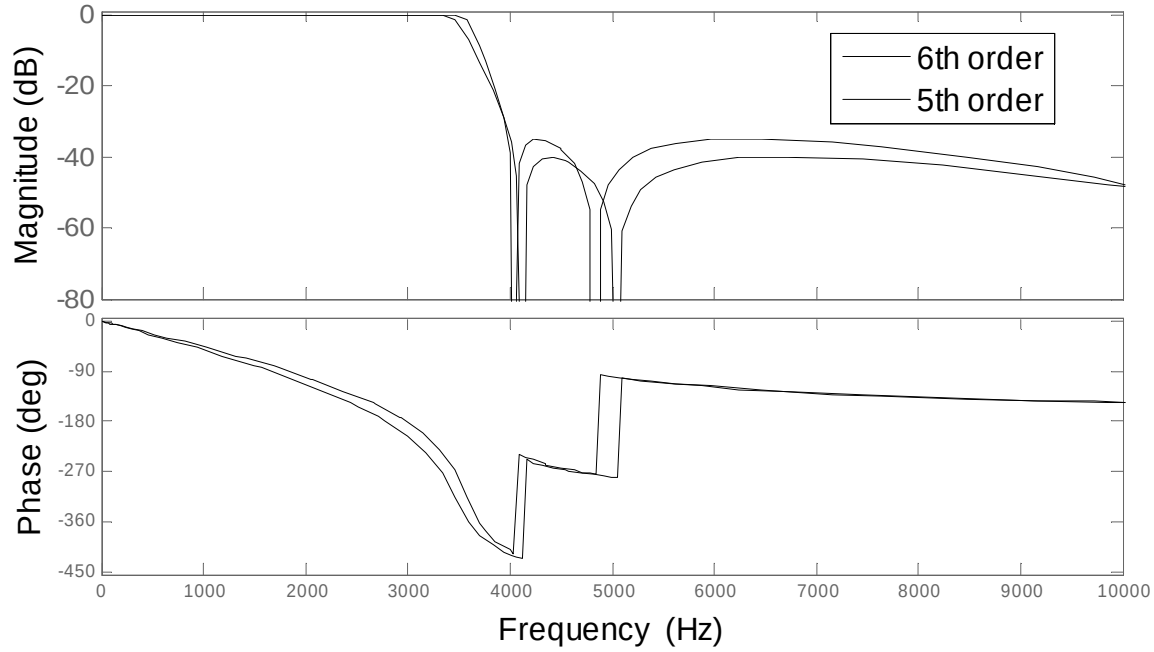


Fig. 5. Frequency Response PCM anti-aliasing filter

frequency SC filter clock together with varying sampling frequency may produce on nonlinear elements of codec and filter undesired products of frequency mixing. Some of them may be located within the filter's passband, so for ANS-DM applications CT filter are recommended. In this paper we describe simulation and experimental results of investigated variants of CT filters dedicated for ANS-DM applications.

Classical PCM filters are useful as input/output filters to the ADM codecs (with the bit rate not lower than 16 kb/s) [4, 9, 11]. Fifth order elliptic low pass PCM filter provides the 3,4 kHz bandwidth. A 50 Hz third order highpass filter completes the transmit filter paths. Receive PCM filter consist of a 3,4 kHz lowpass fifth – order elliptic section and performs band-limiting and smoothing staircase signal. In addition *sinc* gain correction is applied to the waveform to compensate for the higher frequencies attenuation caused by the input capacitive S&H circuit [12, 13]. In this work $1/\tau_{max}$ >16 kHz so *sinc* errors are very low and this block is not implemented.

The output filter should to have a frequency response roll off with minimum slope 40 dB/dec. and stop-band rejection equal or greater than 45 dB [13].

Filter's frequency response specifications are summarized in Tab.2 [13].

For the sake of simplicity, in the project we focused on lowpass filter implementation, assuming that rejection of the 50-60 Hz supply interference, will be considered separately. As a desired approximation of the anti-aliasing filter we have chosen a 5^{th} order elliptic filter (such an approximation is mostly used for SC filters in PCM codecs) and 6^{th} order elliptic filter (a higher order leads to better performance, while an even order of the filter simplifies a little synthesis of the filter when cascading three similar biquadratic blocks).

The magnitude- and phase- frequency response of mentioned transfer function are depicted in Fig. 5

Tab.2. Frequency Response PCM anti-aliasing filter (Relative to 1.02 kHz @ 0 dBm0).

Frequency (Hz)	Min (dB)	Typ (dB)	Max (dB)
15	-	-	-40
50	-	-	-30
60	-	-	-26
165	-	-3	-
200	-1	-	-0.4
300 to 3000	-0.2	-	0.15
3200	-0.2	-	0.2
3300	-0.35	-	0.15
3400	-0.8	-	0
3600	-	-3	-
4000	-	-	-14
4600 to 100 k	-	-	-32

IV. CLASSIFICATION OF INVESTIGATED FILTERS IMPLEMENTATIONS

With respect to applied supply voltage investigated filters may be divided into two basic classes.

1. filters operating at conventional voltage for the technology in question (3-3.3 Volt);

2. filters dedicated for significantly reduced supply voltage (0.7-0.9 Volt)

As mentioned before SC filters mostly use nominal supply, CT filters for single (3-4) kHz range and conventional supply may be implemented in many circuit architectures - and we investigated in more details two of them:

a. RC filters with operational amplifiers (OpAmps);

b. filters with active realization of LC prototype.

To begin let us consider 1a class: to obtain the desired relatively low cut-off frequency a large time constant is required. On the other hand, in order to fit the entire filter into reasonable chip area, capacitors we use are limited to teens of picoFarads. This leads to enormous value of resistors. They may be implemented using HR resistors available in AMS Foundry Design Kit (FDK), but it this case they would occupy the chip area comparable to that of capacitors. Therefore we decided to use active resistors in the form of long channel MOSFETs. This trick significantly reduced the final area of the CMOS chip [14]. For 1b class the design considerations are very similar: assumed limitations for capacitors require the use of inductor coils (or to be more specific their active equivalents) with values of tens to one hundred Henry. The most popular method of coil-less inductance is the use of gyrator. The gyrator [15] is active two-port network described with the admittance matrix equation (6)

$$y = \begin{bmatrix} 0 & g_m \\ -g_m & 0 \end{bmatrix} \qquad (6)$$

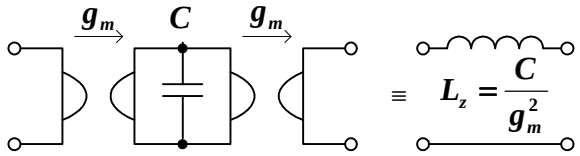
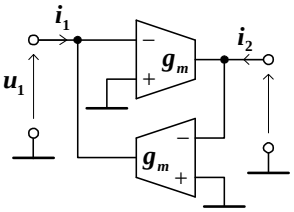


Fig.6. A gyrator equivalent of floating inductor



$$y = \begin{bmatrix} 0 & g_m \\ 0 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -g_m & 0 \end{bmatrix}$$

Fig. 7. A gyrator made of two transconductance amplifiers

Using single gyrator it is possible to obtain a grounded inductor, while for floating inductor (necessary for elliptic lowpass prototype) two gyrators are needed – Fig. 6.

The easiest and most direct gyrator implementation, comprising two transconductance amplifiers is depicted in Fig. 7.

Speech frequency range together with limitations on capacitor values results with very low g_m values. Moreover usually transconductance should be constant within different input signal magnitudes, while the low-power consumption is standard requirement. All these factors cause that the use of subthreshold region of MOSFET is very attractive for the applications in question.

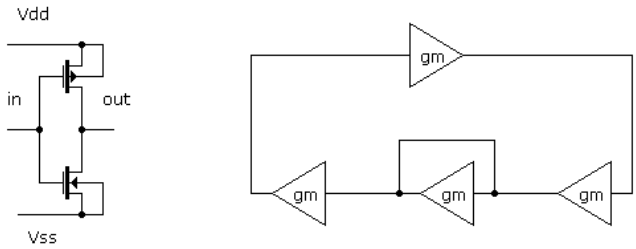


Fig. 8. Gyrator implementation using single input transconductors (e.g. inverters)

Standard supply voltage transconductance amplifiers were based on long tail pairs, since such class of circuit is rather intuitive and no additional active stages are needed to form a gyrator.

Now let us consider the last class of the filters – those working with significantly reduced supply. For supply voltages below 1 Volt (compare this with threshold voltages mentioned in the first section) almost all practical circuits containing the stack of at least two MOSFETs – will have elements working close to the weak inversion (or subthreshold) region. Consequently the design of high or even fair performance operational amplifier seems to be a very difficult if not impossible task. Therefore only gyrator based circuits were of our interest. As a basic building block we used a transconductance amplifier comprising a CMOS inverter only. Gyrators based on such transconductor must have slightly different architecture, since inverter (in contrary do diff-pair) has only one input. Therefore additional stages were necessary. A schematic of inverter working as a transconductance amplifier as well as gyrator implementation for this case are presented in Fig. 8. The middle and shorted transconductor in the lower path works as $1/g_m$ resistor. The use of conventional constant value resistor would not assure the matching of the stages if g_m were changing, while the presented solution guarantees it. Transconductance of single inverter is strongly dependent on supply voltage thus it is very sensitive to any supply changes.

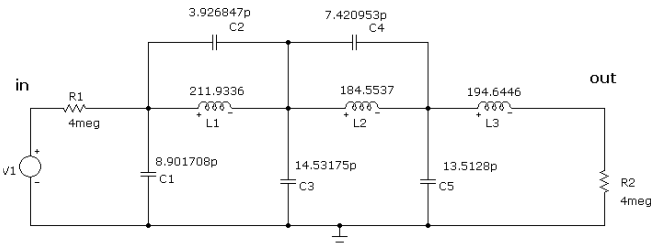


Fig. 9. LC filter prototype

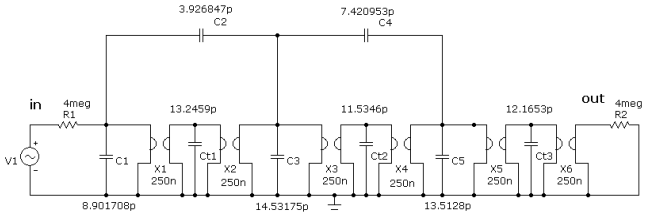


Fig. 10. Active equivalent of LC filter prototype

V. SCOPE OF THE WORK

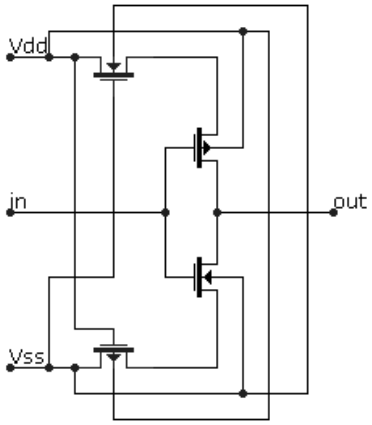


Fig. 11 The schematic of inverter-based transconductor

As we mentioned in introductory section, we investigated 5 circuit solutions of CT filters. Four of them realize sixth order elliptic transfer function and are based on passive prototype showed in Fig. 9 (absolute values of inductors and capacitors are of secondary importance, vital for approximation are only mutual numerical relationships of the elements). To eliminate inductors an equivalent gyrator implementation has been used – see Fig. 10. To assure necessary elements' ratio accuracy, all the capacitors were realized using a matrix of identical unity elements and the desired value were realized by parallel connection of appropriate number of unity elements. The choice of unitary capacitor is subject of subtle trade-off and described in more detail in [11].

An equivalent scheme from Fig. 10 may be implemented using various active elements forming the transconductor. The actual circuit solution comes first of all from assumed supply voltage. For reduced supply (0.7-0.9 Volt) an inverter based implementation is preferred. To achieve desired value of gm (assuming limits for capacitor values) a basic complimentary pair MOSFETs should work in weak inversion mode. For AMS transistors and supply voltages endorsed by electrochemical or photovoltaic sources (0.7, 0.9 Volt) two additional transistors are needed. The full schematic of the transconductor is depicted in Fig. 11. This filter [11, 14, 16] was designed in two slightly different layout variants.

A bit more complicated implementations of schematics from Fig. 5 are based on differential amplifiers with current mirror load [4, 17, 18]. The schematic of a transconductance amplifier based on this concept is presented in Fig. 12. For current range expansion using the same supply voltage a "high swing" variant of current mirrors can be used (Fig. 13).

Another implementation approach (without gyrators) can be classical architecture of active RC filter based on operational amplifiers. This concept can not be realized with reduced supply due to OpAmp supply requirements. We designed a 5^{th} order filter, since this is quite enough to meet PCM standards. The simplified schematic of this circuit is depicted in Fig. 14.

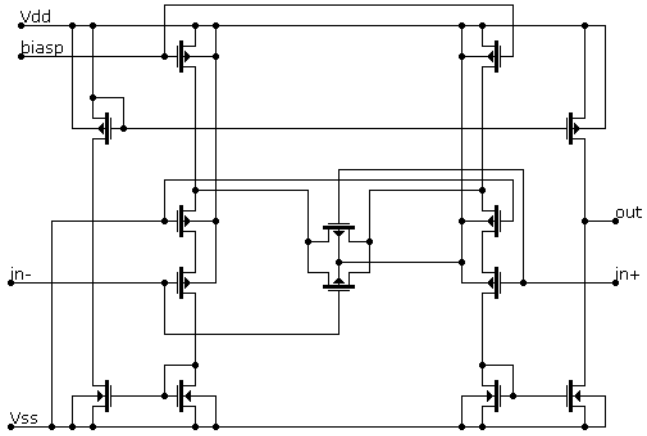


Fig. 12. The schematics of transconductance amplifier with simple current mirrors

Tab 3. Summary of the most important filter parameters

Type of filter / Parameter	LV 1	LV 2	DP	DP HS	OpAmp
Chip area [mm^2]	0.2730	0.2873	0.2730	*0.2907*	**0.1782**
Power consumption [μW]	**max 0.5**	**max 0.5**	32	30	*243*
Passiband ripple [dB]	1.069	1.11	*1.64*	0.4	**0.3**
Average roll-off [dB/kHz]	**-59.2**	-43.8	*-16.1*	-40.4	-27.2
Max current [μA]	**0.55**	**0.55**	1.08	1.0	*81*
RMS iddle noise [μV]	77.6	**55.1**	560.7	*635.1*	180.3

LV1, LV2 – filters based on CMOS inverters, DP – filter comprising differential pair,
DP HS – same as above but with „"high-swing" mirrors

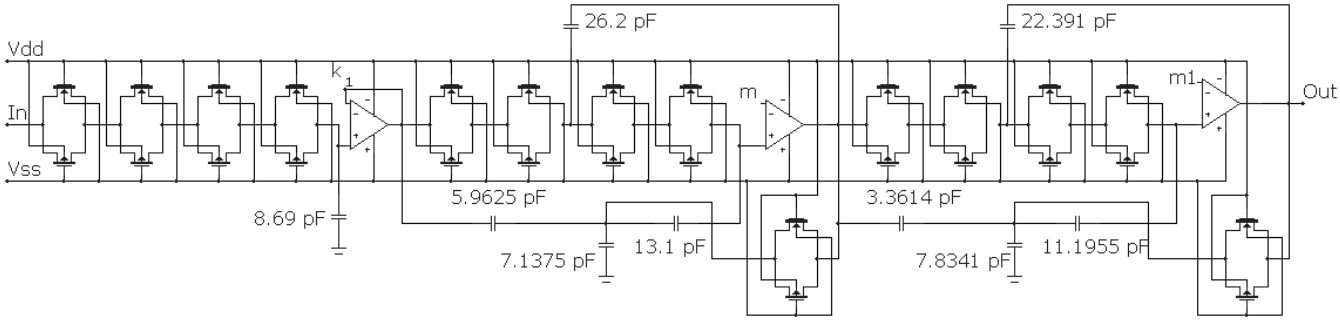


Fig. 14. OpAmp based RC 5th order elliptic filter

VI. The Results

All the filters have been carefully laid out and simulated using BSIM3.3 simulation model for Cadence provided by the silicon foundry.

In Table 3 we summarized the most important figures of merit for investigated filters

The best results are emphasized by bold typeface and the worst ones with italics.

All the gyrator filters occupy similar silicon area, independently on transconductor implementation, while OpAmp based filter fits into significantly lower (about 30%) area.

As expected gyrator filters have very low power consumption. OpAmp based filter power is greater by at least one order of magnitude.

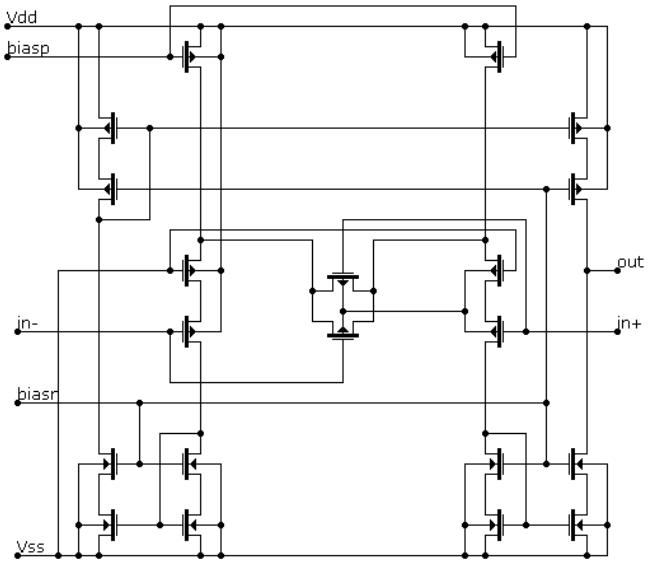


Fig. 13. The schematics of transconductance amplifier with "high-swing" current mirrors.

The worst passband non-uniformity has the DP filter with simple current mirrors. The same transconductor with improver "high-swing" mirrors, is on the other hand, the best, as long as ripple is under consideration. It confirms known good features of high-swing mirrors. OpAmp variant is also very food with this parameter, which comes from simple architecture and high gain stability of feedback amplifiers.

The required roll-off posses all but DP simple mirror filter. In this solution we used the simplest current mirrors and it leads to reduction of current gains in the transconductor and consequently worsening of adjusting input-output circuits efficiency.

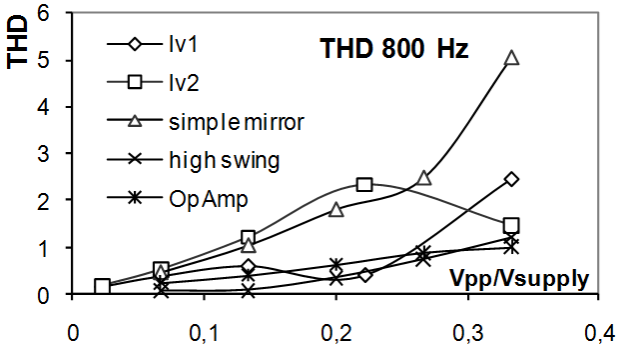


Fig. 15. THD of various filters versus input signal magnitude for 800Hz

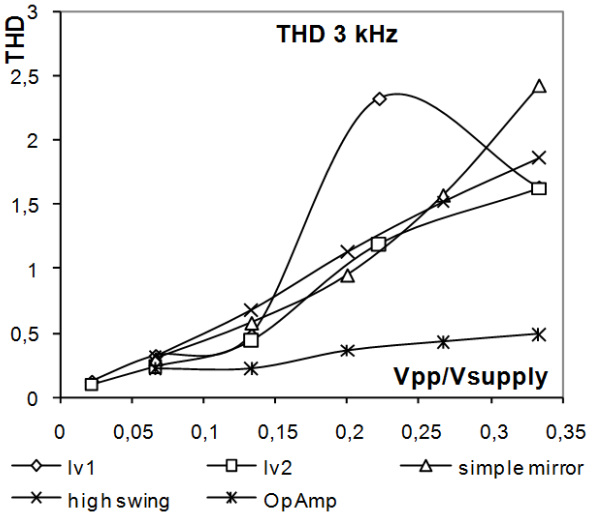


Fig. 16. THD of various filters versus input signal magnitude for 3kHz

All the gyrator filters have the same adjusting resistance (4MΩ). Therefore their idle noise depend basically on current consumption, which is significantly lower for low supply voltage. For OpAmp circuit higher current consumption is caused by appropriate biasing.

Very important parameter for speech filter is harmonic distortion (THD). We estimated and compared this parameter for all the simulated circuits. Simulations have

been performed focusing on two frequencies – basic for speech i.e. 800kHz and harmonics being close to the maximum – 3kHz

As it can be seen in Figs. 15-16 at 800Hz the greatest harmonic distortion occurs in filters working with reduced supply. At 3kHz, on the other hand, the OpAmp filters has the minimal distortion, while LV 2 filter has maximal distortion.

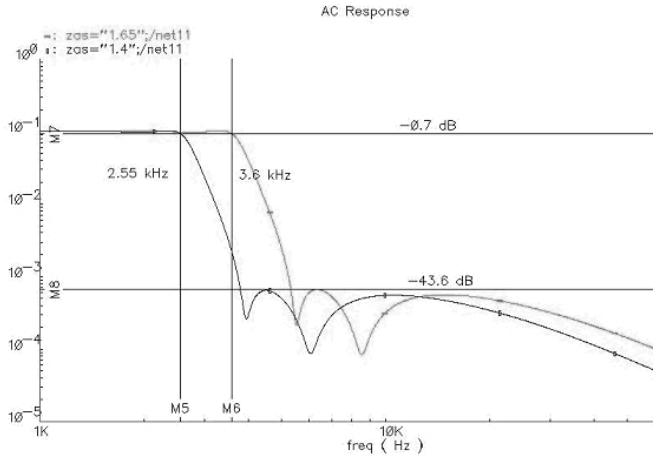


Fig. 17. Magnitude frequency response of 5th order OpAmp based filter for different supply (description in the text)

VII. Tuning properties of implemented filters

Fabrication process variations for single semiconductor devices caused by local and/or global disturbances during fabrication process lead to slight dispersion of filter made in silicon. Therefore some tuning scheme should be provided for every integrated filter.

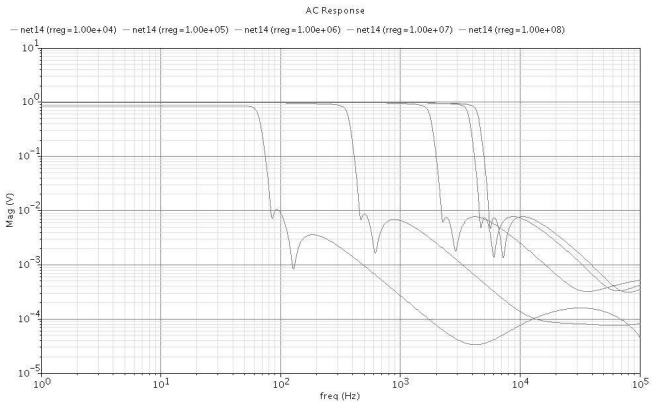


Fig. 18. Tuning range of gyrator lowpass filters based on long tail pairs.

The OpAmp based filters 1.a. may be tuned up within small range by appropriate change of the supply voltage. Fig. 17 shows the impact of supply voltage on frequency response. The supply voltage was increased from 2*1.4 V to 2 *1.65 V. As shown in Fig. 17 the cut-off frequency changes from 2.55kHz to 3.6kHz.

Gyrator filters (both with inverter as well as long tail pair based transconductors -1b,2b) tuning may be performed by transistor's gate voltage variations. This approach is especially effective for gyrator filters with diff pairs. In Fig. 18 the family of frequency response curves is shown. From this figure it comes that maximum tuning range for 1.b. filters cut-off frequency lies between 200Hz and 5kHz.

VIII. Layout of the ANS-DM codec

The filters in question have been implemented in double poly four metal 0.35 μm CMOS technology from austriamicrosystems (AMS). In Fig. 19 we present the layout.

Total chip area of the circuit with I/Os shown in Fig. 19 is 3 sqmm, while the core is 1 sqmm only. From Fig. 19 it is apparent that most of the core area (79%) is occupied by the filters. On the other hand in single filter the great majority of silicon area (75%) is consumed by capacitors, active circuitry is only 25% in terms of area.

IX. Conclusions

The results presented in the paper extend the state-of-the-art and contribute a little to implementation of sampling adaptation concept, both in analytical and practical aspect.

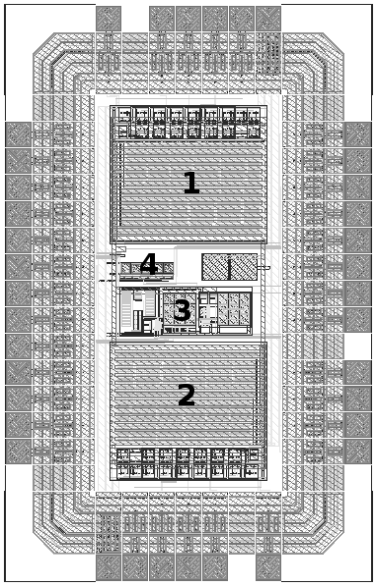


Fig.19. Layout of the ANSDM codec with marked following arrangements: 1. Input filter, 2. Output filter 3. Integration module, 4. Comparator

We illustrated the concept of the delta modulator/demodulator realization with the aid of the non-uniform sampling method. All elements, both analog and digital, that are used for this implementation, can be put together in one chip, making ASIC/SoC dedicated to special purpose, such as: measuring, communication, control systems, data compression, data encryption wireless telecommunication.

In the paper we described modulation the ANS-DM algorithm implementations, the codec architecture but we focused on filtering aspects and filter implementation in CMOS technology.

The results and analysis of the filters presented in the previous section lead to some vital conclusions:

The filter with transconductor realized with simple current mirrors has definitely the worst performance;

Reduced supply voltage variants of gyrator filters fulfill all the PCM requirements. In practical realization, however, their tendency to introduce nonlinear distortion should be taken into account;

The "high swing" circuit fits into specifications with all but idle noise. This is result of high current consumption and a special attention must be paid on this parameter;

The OpAmp circuit is especially well suited to high linearity applications and has the smallest silicon area. This benefits are however paid by highest power consumption.

As we mentioned all the circuits have been manufactured and systematic experimental test are currently in progress.

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