Capacitor-less Low-Dropout Regulator for Analog Sensing using 90nm Technology

Pavan M S[1]
Department of Electronics & Communication,
Ramaiah Institute of Technology, MSR Nagar, MSRIT Post,
Bangalore-560054, Karnataka, INDIA
e-mail: pavanachar28@gmail.com

M Nagabushanam[2]
Department of Electronics & Communication,
Ramaiah Institute of Technology, MSR Nagar, MSRIT Post,
Bangalore-560054, Karnataka, INDIA
e-mail: nagabushanam1971@gmail.com

Sushmita Hawaldar[3]
Department of Electronics & Communication,
Ramaiah Institute of Technology, MSR Nagar, MSRIT Post,
Bangalore-560054, Karnataka, INDIA
e-mail: sushmitahawaldar@gmail.com

S L Gangadharaiah[4]
Department of Electronics & Communication,
Ramaiah Institute of Technology, MSR Nagar, MSRIT Post,
Bangalore-560054, Karnataka, INDIA
e-mail: gdhar75@gmail.com

Received: March 27, 2021. Revised: August 1, 2021. Accepted: August 27, 2021. Published: August 30, 2021.

Abstract— The capacitor-less-output-low-dropout (CLO-LDO) regulator proposed in this study can manage a wide variety of load currents. To offer temperature independent controlled LDO output, the LDO's 0.844V reference voltage is obtained using BGR, the optimized design is presented that provide full range stability, fast transient response. These benefits allow the proposed LDO regulator to operate over a wide range of operating circumstances, with very high current efficiency 99.99% and low voltage drop 100mV, operating using very low quiescent current of 0.02µA, at the output of regulator. The proposed regulator design is constructed in 90nm CMOS technology, the structure of the regulator is implemented using a Two-stage operational amplifier to obtain large DC gain 50dB to improve supply noise rejection, and a feedback loop, and exhibits better performance in terms of large phase margin 64.516 degrees with no load and 70.63degree full load.

Keywords—Band gap reference (BGR), Capacitor-less, Complementary to absolute temperature (CTAT), Low-dropout (LDO) regulator, Proportional to absolute temperature (PTAT).

I. Introduction

In recent years, battery-powered portable electronic gadgets, such as cameras, PDAs, mobile phones, and other palm-sized devices, have become quite popular in recent years. The number of advanced electronic devices is decreasing, but battery efficiency numbers are increasing, which might be a calculation for stretching the limitations of control administration frameworks. Power management is vital for these batteries prepared devices since once the battery control begins depleting and the effectiveness of these devices decreases with time. Power management very critical for these battery-powered gadgets like the DC-DC converters, linear voltage regulators, switching regulators and LDOs which are all part of the power management system.

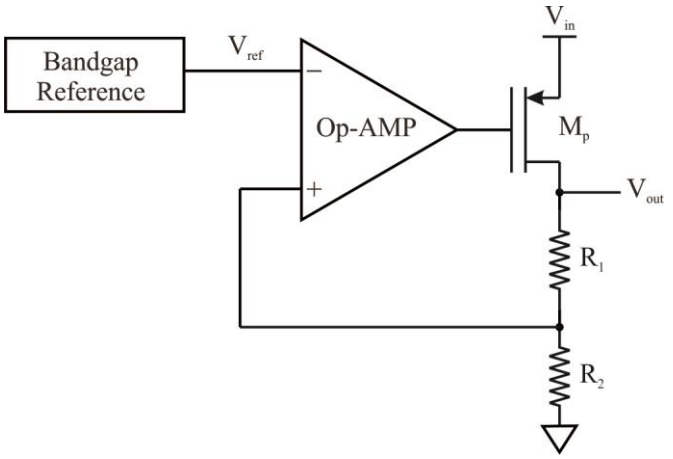

Fig. 1 Conceptual schematic of the proposed capacitor-less regulator

Voltage regulator is intended for analogue front-end circuits that may require very little power. Fig. 1 illustrates the schematic of an energy-autonomous-sensing system with energy-harvesting-circuitries and a reconfigurable-analogue-sensing circuit. The challenge of designing a low quiescent current, wide output current range LDO in a mainstream CMOS process has two objectives:

1. The power MOSFET's leakage current must be large enough to generate the peak load current.
2. Low power analog design usually leads to greater parasitic. Combined with the need for a large pass element, the compensation of the LDO proves difficult [1].

A linear voltage power efficient regulator, which converts the fluctuating voltages generated by the switching converters right into a unique and quiet supply voltage, efficient regulators are basically needed to save susceptible physiological signals from being smeared by supply ripples. A voltage-controlled current source is used in a linear regulator to ensure that a constant voltage is maintained at the regulator's output. The circuit's control block regulates this voltage by properly supplying controlled voltage to a voltage-controlled current source, and it should always keep track of the output voltage in order to maintain the output voltage at the regulated constant value [2].

The conventional LDO consists of an error amplifier, a pass PMOS transistor, feedback network (R1 and R2), the parasitic capacitances namely Cgs and Cgd of the pass element included for frequency analysis, by breaking the feedback loop as shown in Fig. 2.

The small signal model of the proposed LDO is shown in Fig. 3, with gm1 representing the trans-conductance of Op-Amp or error-amplifier and g_{mp} the trans-conductance of pass transistor. Rout1, Cout1 are the output impedance and load capacitor of op-amp respectively whereas Rout2 and capacitive load (CL), at output of LDO are the output impedance and on-chip load capacitive respectively.

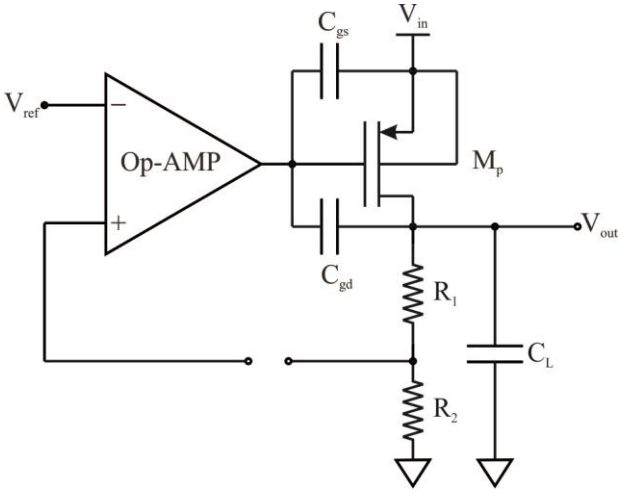

Fig. 2 Proposed Capacitor-less regulator with loop break-up

At the node of potential divider R1 and R2 the voltage is V_3 in terms of LDO output is shown in equation (1), where the feedback fraction is represented by β and is given by equation (2), using the small signal model for the frequency analysis as shown in Fig. 3, we obtain the number of poles and zeros for the proposed LDO.

$$V_3 = \beta V_{out} \tag{1}$$

$$\beta = \frac{R_2}{R_1 + R_2} \tag{2}$$

By applying KCL at node V_1 and V_{out} we obtain two equations

$$-\frac{V_1}{R_{out_1}} - SCgdV_1 - SC_{out_1}V_1 + SCgdV_{out} = -gm_1V_2 \tag{3}$$

$$gm_pV_1 - SCgdV_1 + \frac{V_{out}}{R_{outeq}} + SCgdV_{out} + SC_{Leq}V_{out} = 0 \tag{4}$$

$$C_{Leq} = \frac{SC_L}{1 + SR_{eL}C_L} \tag{5}$$

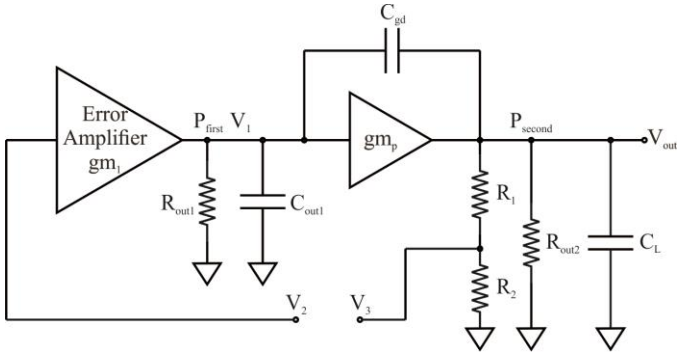

Fig. 3. Proposed capacitor-less regulator Small-signal circuit

By combining equations (3) to (5) the transfer function of LDO is given in equation (6)

$$G(S) = \frac{-\beta gm_1 gm_p R_{out_1}\left(1 - S\frac{Cgd}{gmp}\right)\left[R_{out_2} \parallel R_1 + R_2\right]\left[1 + SC_LR_{cL}\right]}{\left\{1 + SC_L\left(R_{cL} + R_{out_2} \parallel (R_1 + R_2)\right)\right\}\left[1 + S\left(cgs + gmpR_{out_2Cgd}\right)R_{out_1}\right]} \tag{6}$$

From the transfer function (6) there are two poles and two zeroes located in a LDO schematic where the first dominant pole is given in equation (7)

$$P_{first} = \frac{1}{\left(R_{cL} + R_{out_2} \| \left(R_1 + R_2\right)\right) C_L} \quad (7)$$

The second dominant pole is given in equation (8)

$$P_{second} = \frac{1}{\left(Cgs + gmpR_{out_2} Cgd\right) R_{out_1}} \quad (8)$$

When the capacitive load C_L is low, the dominant pole moves towards high frequency, if the C_L is high the dominant pole moves towards low frequency. The non-dominant second pole depends on the impedance of error amplifier and output capacitance therefore the frequency response and stability depends only on C_L & C_{out}.

II. Literature Review

Globally, great efforts are being made to develop VLSI systems such as converters, linear regulators and switches which are among the most volatile and dominant systems today in terms of stability and energy efficiency. This section provides an overview of the research work developed in recent years to achieve better converter design. Huang, ChungHsun, YingTing Ma, and WeiChen Liao, [3] adopted a basic symmetric active transmission amplifier used as error amplifier, with the concept of current separation to increase gain, which improves LDO controller closed loop bandwidth. In the output stage of the rail-to-rail error amplifier, a noise power cancellation mechanism is formed; size of the power MOSFET can be minimized. In addition, a transient fast response accelerator is identified through the reuse of error amplifier parts. These foci allow the suggested LDO controller to work in a variety of environments. While achieving fast transient response with low voltage, low quiescent current and high PSR under a wide range of operating condition motions. Tan, Yi, Chenchang Zhan, and Guanhua Wang, [4] Constructs a full-on-chip-analog regulator for low voltage applications, regulator with a negative charge pump is used. This design uses a negatively charged pump as the ground of the controller to provide additional voltage range to the error amplifier and power transistors, which allows very efficient and precise tuning below the power supply. The supply voltage is limited. The proposed design can accept an output current of 1μA at 45mA with a voltage drop of 100mV below 0.6V at the input with a quiescent current of 21μA. Joshi, Kishan, Sanjeev Manandhar and Bertan Bakkaloglu, [5] Bipolar / CMOS / DMOS (BCD) technology implementation with instantaneous response at fast charge with 6.1s recovery time and quiescent current of 5, 6A and achieve a PSR above 68dB up-to 2 MHz frequency and over a wide load range up-to 250mA. Wideband PSR is achieved using a Current Direct Acting Ripple Amplifier (CFFRC) which improves PSR by up to 25dB. The CFFRC amplifier makes the difference in achieving low static power. Bautista and Meriam Gay, [6] suggest a 1.8V supply, 50mA current, and a single compensation capacitor from a 1pF LDO regulator. The maximum output load current is 50mA at the specified output voltage of 1.68V. The LDO PSRR rating is 73dB at 16.7 MHz and relatively low power at 90mW. The voltage regulator provides full load transient response of 3.4mV overshoot and 5.5 mV overshoot. Motkurwar, Supriya and Ujwala Ghodeswar, [7] presented a gain approach in LDO with high load regulation designed by 90nm CMOS technology, achieving a PSRR of over 70dB up-to 100 KHz for load current up-to 100mA. The voltage regulator provides a maximum load current of 110mA with a supply voltage of 1.2V providing 1V output with a voltage drop of 200mV. Alapati, Suresh and Sreehari Rao Patri, [8] presented a no-load 1.5μA quiescent current-consuming LDO designed with 180 nm CMOS technology. It displays fast stabilization times, low quiescent currents, less hysteresis and adaptive capacitors. The topology includes a through-segment transistor with ground modulation and adaptive bias current control stages for enhanced transient performance. This arrangement further improves the resolution time to 1s internal while limiting the overshoot to 171mV / 82mV to switch the load current between 0 and 100mA with a 40pF load capacitor.

TABLE I. Summary of Literature Review

Design Parameters	[3]	[4]	[5]	[6]	[7]	[8]
Technology (CMOS)	90nm	65nm	180nm BCD	180nmm	90nm	180um
VIN/VOUT(V)	1/0.8	0.6/0.5	5/5.25	1.8/1.68	1.2/1	1.8/1.66
Load capacitor CL(μF)	1	0.1	2.2	-	0.1	40p
Maximum IQ(μA)	60	21	35.6	4.41	26	1.5
Maximum Iout(mA)	100	45	250	50	-	100
Current efficiency (%)	99.94	99.95	-	93		99.89
Load regulation(mV/mA)	<0.24	0.047	0.112	2.16	222	0.104
Response time TR(μs)	<0.25	-	-	-	-	-
PSR@100kHz(dB)	>50	-	-	-72.13	-70	-36.18
Area(mm2)	0.8	0.045	0.12	-	-	-
Dropout voltage(mV)	200	100	250	120	200	200

The literature summary in Table I shows that the proposed regulators employ a basic operational amplifier to achieve high gain and noise cancellation capabilities; however, with different nodes of technology, a linear regulator is implemented, resulting in increased power consumption and lower current efficiency; however, these are minor drawbacks that leave room for further architectural improvement in terms of area, stability, and efficiency. To prevent the usage of any

off-chip capacitor on the output side, a capacitor-less low-dropout regulator was proposed, which saves a lot of space and improves power efficiency [9]. The proposed design's major purpose is to improve the regulator's stability without using any off-chip capacitors.

Section II addresses the specifications for the suggested design to fulfill the desired dropout voltage and excellent stability, which are derived from the literature overview, Section III discusses the proposed basic concepts of LDO's, and difficulties in implementation. The design of LDO sub-blocks such as the Error-Amplifier, a feedback network, a Band-gap reference circuit, and a power MOSFET is covered in Section IV. Section V addresses the complete integration of all sub-blocks, as well as simulated measurement outcomes, Result analysis are discussed in section VI and the conclusion is presented in section VII.

III. Design Challenges and Concepts of the Proposed Low-Voltage-LDO-Regulator

A band-gap reference circuit (BGR), an error-amplifier (EA), a power MOS transistor (MP), and a feedback network are the four major components of an LDO regulator. Some of the suggested LDO's improved performance characteristics will be discussed in the following sections.

A. Low Dropout Voltage and Low Quiescent Current (I_Q)

The voltage difference between the input and output voltage required for regulation to occur is specified as the dropout voltage of an LDO. The current absorbed by the internal circuitry when it is active is known as quiescent current. Both the dropout voltage and quiescent current values for a good LDO should be extremely low. The circuit's maximum load current determines the dropout voltage. As a result, the maximum load current should be as low as feasible in order to achieve very low dropout voltage [10].

B. Power Supply Rejection

It is defined as a capability of an electronic circuit to have a constant and precise output voltage even with the power supply variations. The proposed LDO architecture is made up of two levels of Error Amplifier. The Error Amplifiers first stage reduces power noise, while the second rejects common mode noise at its inputs. Power supply rejection can be increased by increasing the open-loop gain of the two-stage op-amp and decreasing the gain from input to output. In-order to improve the power supply rejection gain of two stages, 50dB is chosen for design [11].

C. Stability

A closed-loop feedback mechanism is referred to as a regulator. The phase margin must be positive for the LDO to remain stable. In other words, the phase of the system should be positive at the gain curve's unity gain crossover frequency. At low frequencies, the power MOSFET (MP) adds a non-dominant pole [12]. This non-dominant pole should be cancelled for stability, and a large CL (RSER) equivalent series resistance should be utilized to achieve a low frequency zero.

IV. Design of Proposed Circuits

A. Error Amplifier

A reference voltage, an error-amplifier, and a power-pass-element, such as a MOSFET, make up an LDO. To regulate the output voltage, the error amplifier offers dc gain. The PSRR is largely determined by the ac gain of the error amplifier. Because the driving strength of the power PMOS block is increased to produce a high PSRR and high gain op-amp, the aspect ratio required for the power MOSFET is reduced due to the greater swing output from the op-amp, necessitating the usage of a two-stage operational amplifier. Fig. 4 depicts a schematic of the Error-amplifier.

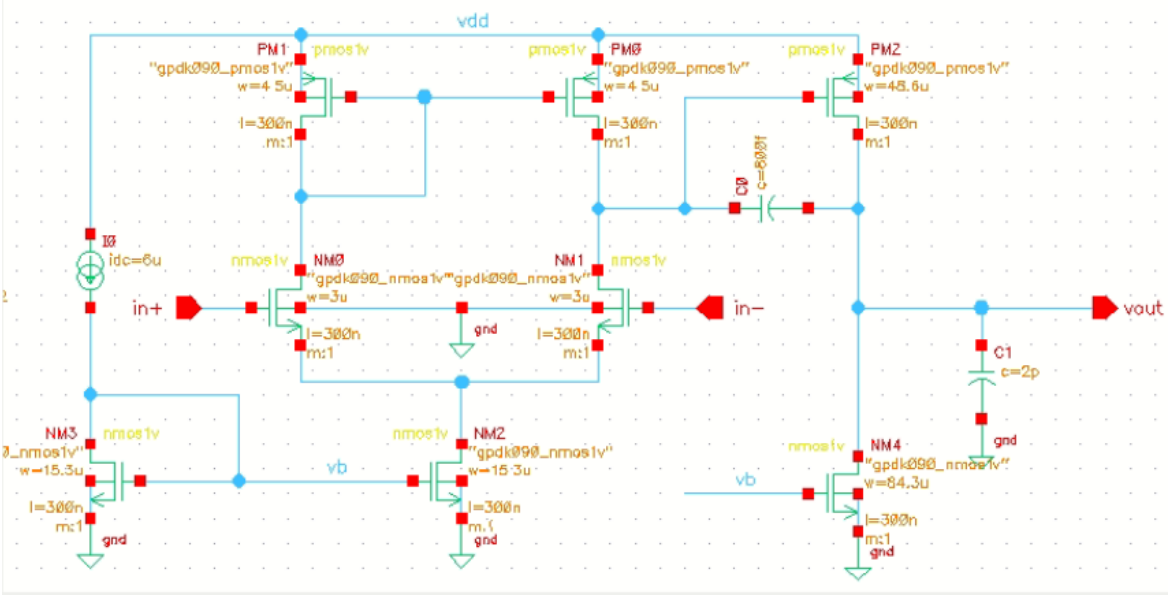

Fig. 4 Schematic of Error-amplifier

The first stage of the Error-amplifier is a differential-amplifier; second stage is the common-source amplifier cascaded to improve the gain. Here with a view to achieve the phase-margin of amplifier greater than 60deg the compensation-capacitor is chosen as 800fF. The NM0 and NM1 are matched transistors and are designed through first choosing the transconductance of NM0 and NM1 as 130µ to achieve high- gain- bandwidth- product. Similarly, the PM0 and PM1 are matched transistors and are designed using the high input- common-mode- range- parameter [13]. By knowing the bias current for the circuit I_{bias} transistors NM2-NM4 are designed. The first stage of the op-amp has a dc-gain of 33dB, which is significantly less than the needed gain. As a result, the second stage comes into play. An overall gain of 50dB and a phase margin of 71deg are achieved in the proposed two-stage op-amp, as illustrated in Fig. 5.

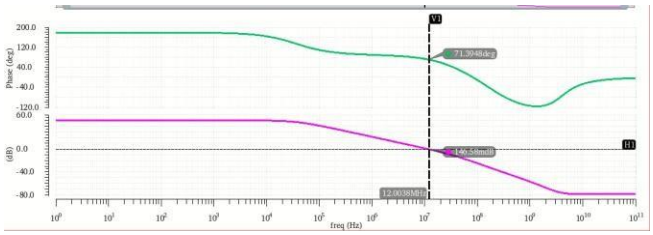

Fig. 5 Gain and phase plot of error amplifier

B. *Band-gap Reference Circuit*

Any integrated circuit must work throughout a large temperature range, ranging from deserts to the north pole regions, which necessitates the use of a constant reference voltage that is unaffected by temperature. As a result, this block is utilized to give a consistent reference voltage to the LDO that is independent of temperature and supply voltage. By using this constant reference voltage, the LDO regulator generates a regulated voltage which can also be a voltage that is independent of temperature [14].

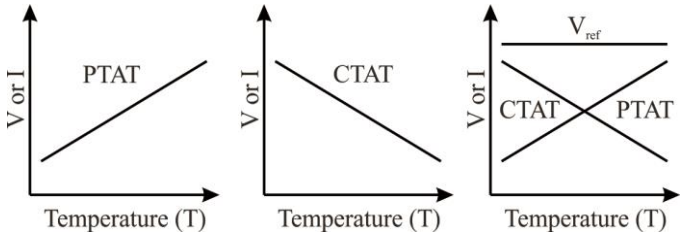

Fig. 6(a) PTAT curve (b) CTAT curve (c) Corrected PTAT & CTAT curve to generate constant voltage reference V_{ref}

The voltage difference between the two p-n junctions produces a current that is proportional to the absolute-temperature (PTAT) in the resistor. This current is used to generate a voltage across the second resistor. This voltage is then added to one of the junctions' voltages. The voltage on a constant current DC diode is analogous to absolute temperature (CTAT). If the ratio of the first and second resistors is suitably chosen, the first-order effects of the temperature-dependency of the diode and the PTAT current will be cancelled, resulting in a constant voltage [15].

Power efficiency and circuit size are significant considerations in the design of band-gap references. Because the band-gap reference is commonly made out of BJT devices and resistors, the overall circuit size can be quite large, resulting in a high design cost. To achieve the appropriate noise and precision specifications, this type of circuit may consume a lot of power. The band-gap reference circuit generates a constant voltage that is independent of supply voltage and temperature. It's difficult to have a constant reference voltage in practice because almost all of the factors change with temperature [16]. However, we must identify two voltage quantities: PTAT, which is proportional to absolute temperature and CTAT as shown in Fig. 6, which is complementary to absolute temperature, in order to have temperature independent voltage.

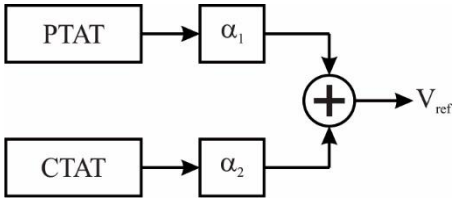

Fig. 7 Concept of BGR

$$V_{ref} = PTAT + CTAT \tag{9}$$

$$V_{ref} = \alpha_1 V_{PTAT} + \alpha_2 V_{CTAT} \tag{10}$$

When these two voltages are added together with some suitable coefficients as shown in the equations (9&10), the result is a voltage that is temperature independent, as illustrated in the Fig. 7. This is because the slopes of two voltages with respect to temperature cancel out, resulting in a voltage with a constant slope or no slope with regard to temperature.

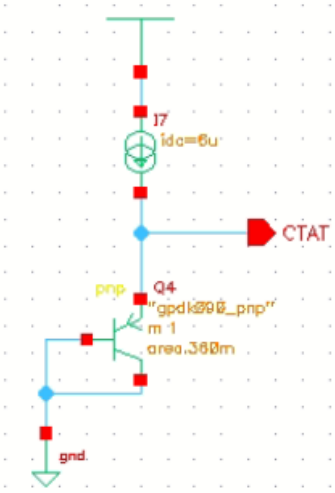

Fig. 8(a) Schematic of CTAT

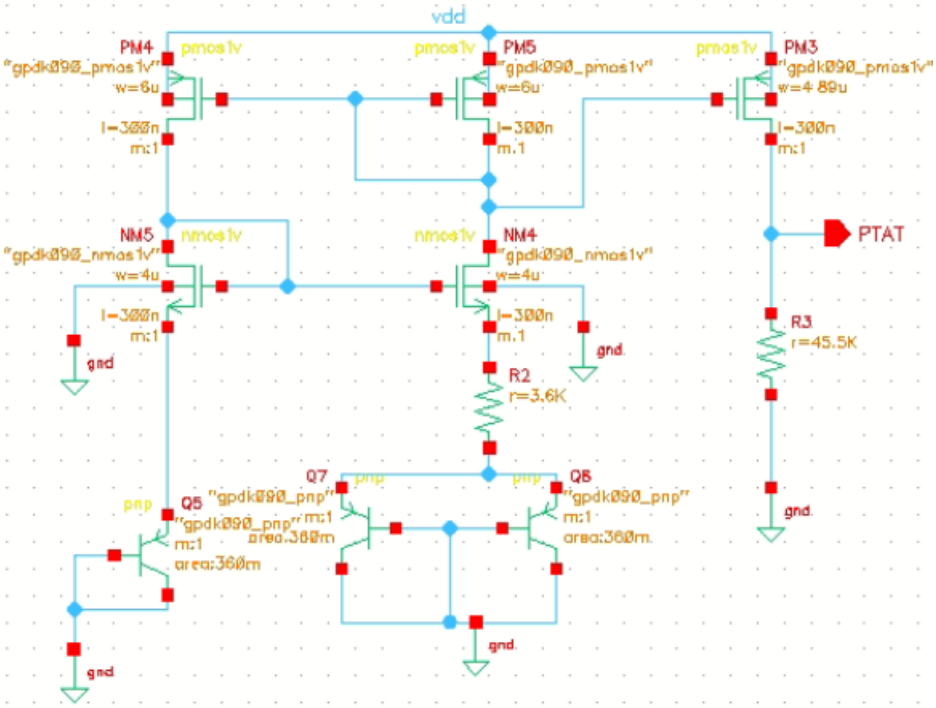

Fig. 8(b) Schematic of PTAT

The creation of various integrated circuits with low temperature drift has resulted from the development of voltage references with low output voltages based on silicon's band-gap voltage. The relative simplicity of the band-gap reference approach, as well as the elimination of zeners and its associated noise, makes it appealing in Integrated-Circuit designs [17]. However, in these current days of ever-dwindling system supplies, the fact that band-gap devices work at low voltages of 1.2V or less is critical. They are employed in the designs of many data-converters, in addition to being used as stand-alone IC references. In this project, a basic BGR is developed to provide an 840mV reference voltage. The BGR design is depicted schematically in Fig. 9.

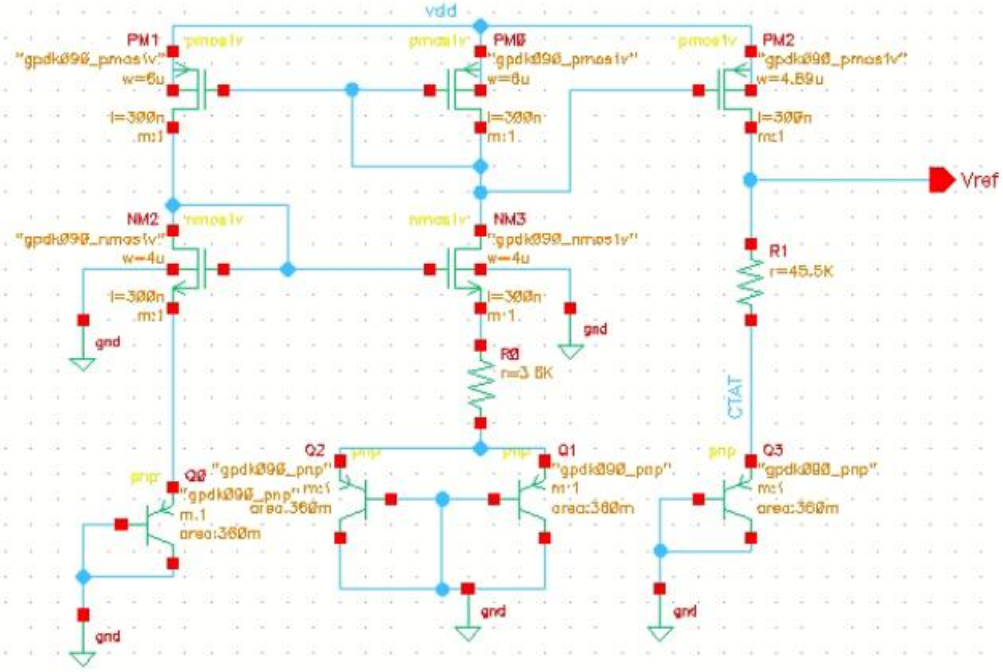

Fig. 9 Schematic of Band Gap Reference

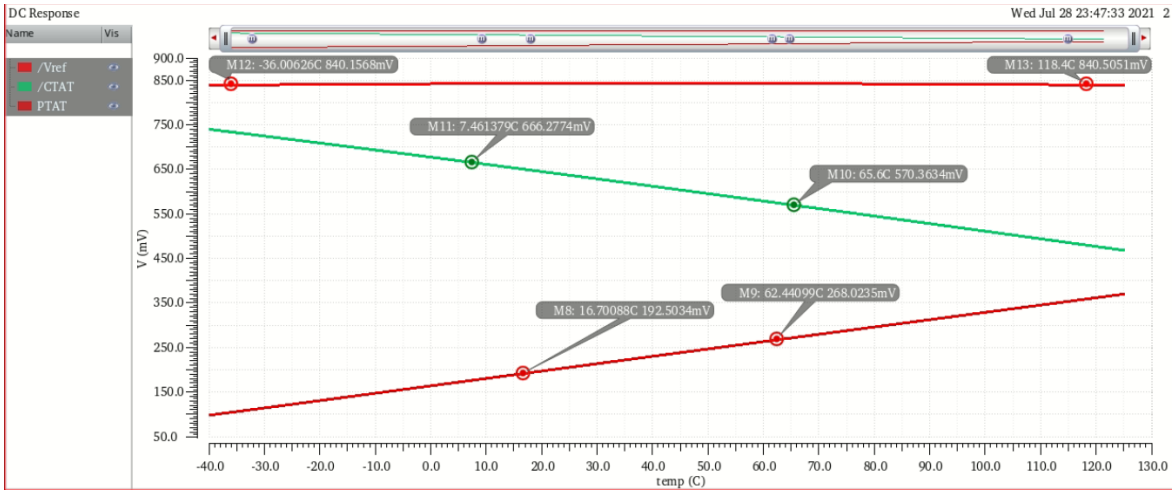

Fig. 10 Output plots of PTAT, CTAT and V_{ref}

C. Power MOSFET

To achieve low-drop-out-voltage, LDO has traditionally used pMOS pass transistors. The error-sensing-amplifier adjusts the output voltage of the LDO by adjusting the gate voltage of the pMOS pass transistor when the load current varies. It is vital to construct an error-amplifier with a wide-bandwidth at the expense of power consumption for fast transient response. This method employs a high aspect-ratio-power-MOSFET. The power MOSFET's aspect ratio is determined by the maximum load current and dropout voltage requirements. To get a lower-dropout-voltage, only a little amount of load current is used. For the above specification, the aspect-ratio may be computed using equations (11&12):

$$V_{dropout} = \sqrt{\frac{2I_{\max}}{\mu C_{ox}\left(\frac{W}{L}\right)_p}} \tag{11}$$

$$V_{dropout} = V_{in} - V_{out} \tag{12}$$

For the specified Power MOSFET, the resultant aspect ratio is 1600, and the specifications are tabulated in Table II.

TABLE II. DESIGN VALUES FOR POWER MOSFET

Parameter	Value
Technology	90nm
V_{DD}	1.2V
Dropout voltage, $V_{dropout}$	100mV
Maximum load current, I_{max}	1mA
M_pC_{ox}	175.104µm

In an LDO, a nMOS transistor can also be adopted as the pass transistor. Although the nMOS pass transistor method provides superior line regulation and transient performance, it has a low power efficiency than the pMOS pass transistor LDO. Also, to enable the nMOS pass transistor the error-amplifier output voltage as well as the supply voltage, should be one VGS higher than the LDO output [18].

D. Feedback Network

Negative feedback is used by the LDO to adjust its output voltage. When the phase of the signal is used to detect changes in the output voltage (VOUT) it delays by 180°.The output voltage oscillates, changing negative feedback into positive feedback. An error amplifier, a drive circuit for an output transistor and the output transistor are all included in the LDO. Due to the capacitance and resistance of these circuits, the feedback loop has an inherent delay [19]. When the phase delay due to this inherent delay approaches 180°, negative feedback transforms into positive feedback, amplifying the difference between the output and reference voltages. Two resistors, R_1 and R_2, make up the feedback network on the LDO's output side. These two resistors are constructed by taking into account the reference voltage from the band-gap reference circuit as well as the needed regulated output voltage.

$$V_{out} = \frac{(R_1 + R_2)}{R_2} * (V_{ref}) \tag{13}$$

TABLE III. DESIGN VALUES FOR FEEDBACK NETWORK

Parameters	Values
R_1	1-356Ω
R_2	844Ω
BGR V_{ref}	844mV
V_{out} Range	0.85 – 1.35

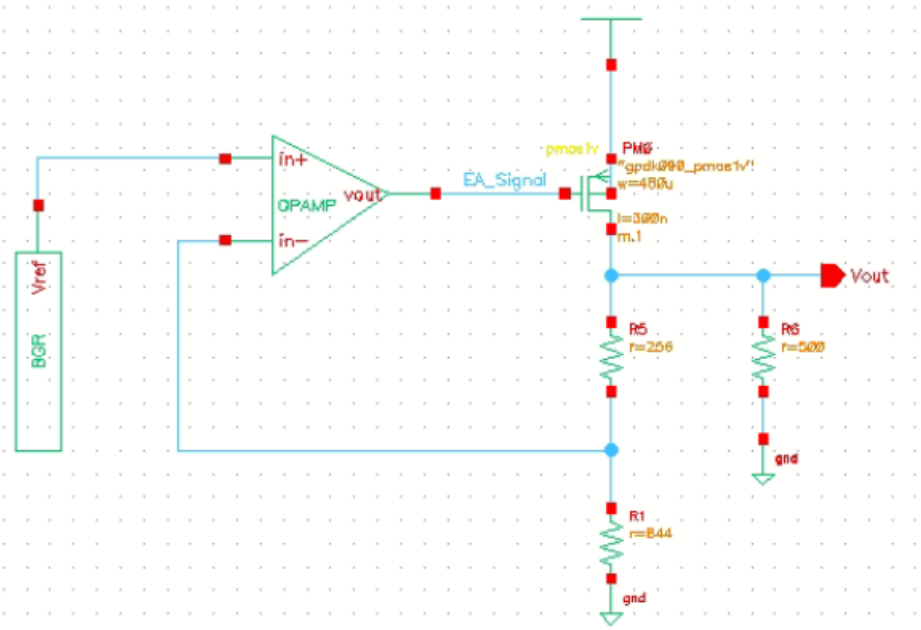

Fig. 11 Schematic of proposed LDO

V. Circuit Realization and Simulation Results

Fig. 11 depicts the proposed LDO regulator's schematic, which includes all of the intended components, such as the error amplifier, feedback network, BGR, and power MOSFET. On the output side, it has one branch with a resistor and a capacitor to improve the circuit's stability. It also has a load resistor RL for output voltage load control. In this circuit, the aspect- ratio (W/L) of Mp is chosen to be 480µ/0.3µ in a 90nm Standard CMOS process where Mp's threshold voltage |Vthp| is roughly 219mV to supply 1mA load current with 100mV dropout.

The dropout value for the provided supply is roughly 100mV, i.e., the output voltage of the LDO for 1.2V of input supply is 1.10072V, with an error amplifier output voltage of 840mV, which regulates the operation of the pass transistor or power MOSFET Mp, as shown in Fig. 12.

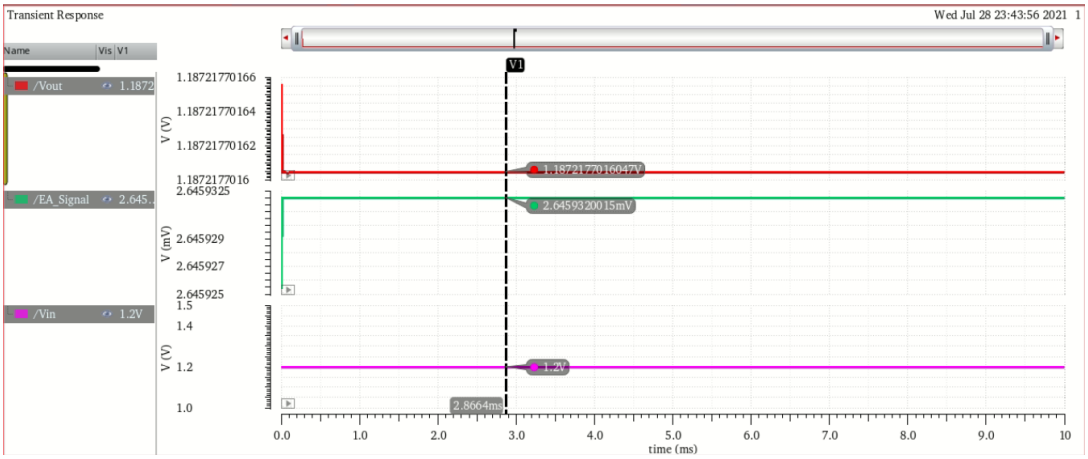

Fig. 12 Transient response of LDO

The Fig. 13 illustrates the output of the LDO simulation waveform when VDD is swept from 0 to 1.5V; it demonstrates that when the input voltage is 1.2V, the output voltage stabilizes at 1.1009V.

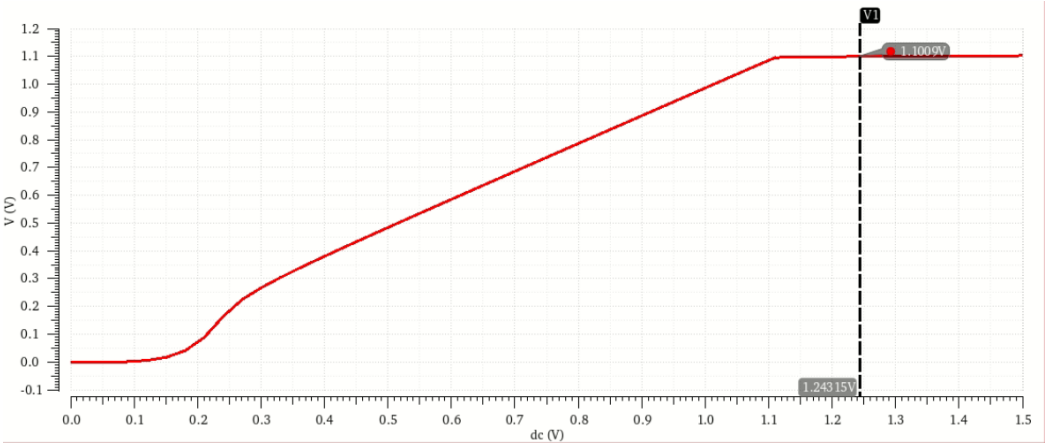

Fig. 13 Simulation waveform of the LDO output when VDD is sweep from 0 to 1.5V

A. *Stability Analysis*

Almost all voltage regulators have a feedback loop to maintain a steady output voltage. For the loop voltage regulator to be stable, the output capacitor must be connected from V_{out} to ground. To do a stability study, we must first break the loop so that no closed loops remain [20]. We utilize iprobe in cadence to break the loop and perform stability analysis. Fig. 14 and Fig. 15 demonstrate the phase margins of LDO with no load and full load, respectively.

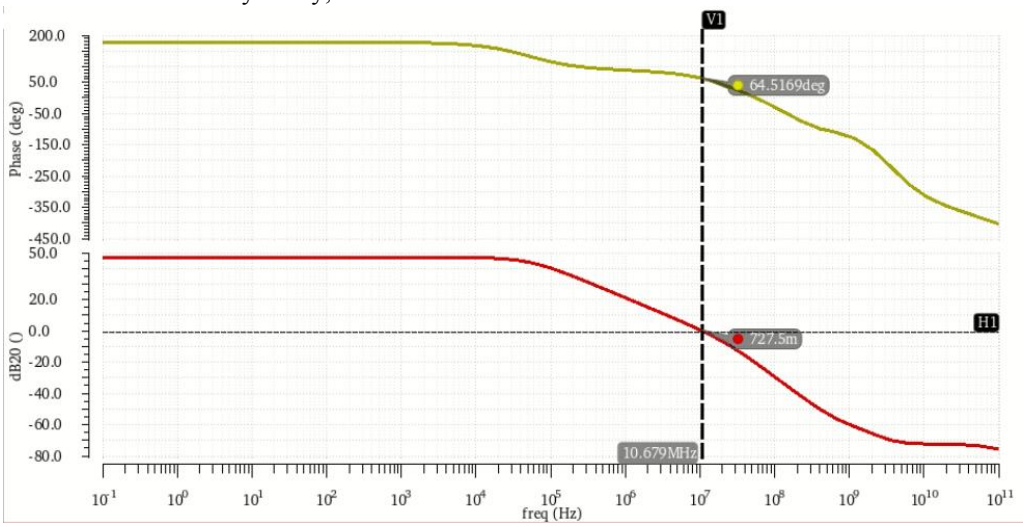

Fig. 14 Phase margin plots for LDO with no-load

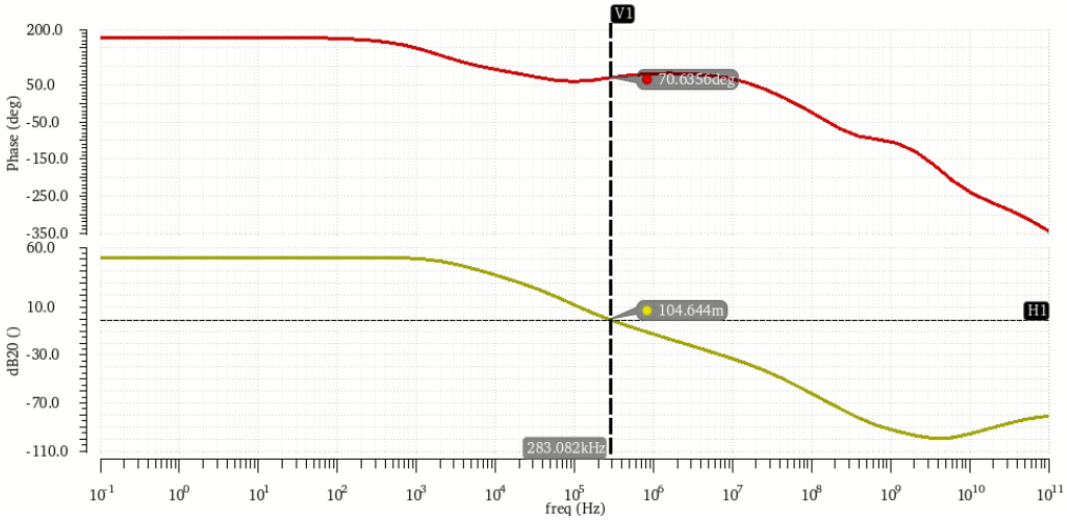

Fig. 15 Phase margin plots for LDO with full-load

B. *Poles and Zeros*

The values of the poles and zeros of a framework determine or not the system is stable, as well as how the system functions. PZ (pole-zero) analysis is used to figure out where the poles are located and how stable the system is. Pole-Zero plots is shown in Fig. 16 & 17 where we can observe the poles are there in left half of plane concluding that the system to be stable.

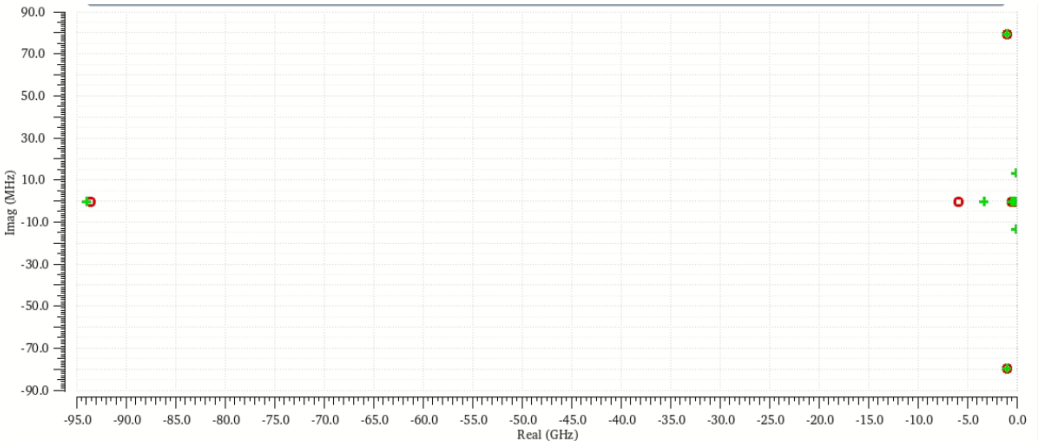

Fig. 16 Pole zero plots for LDO

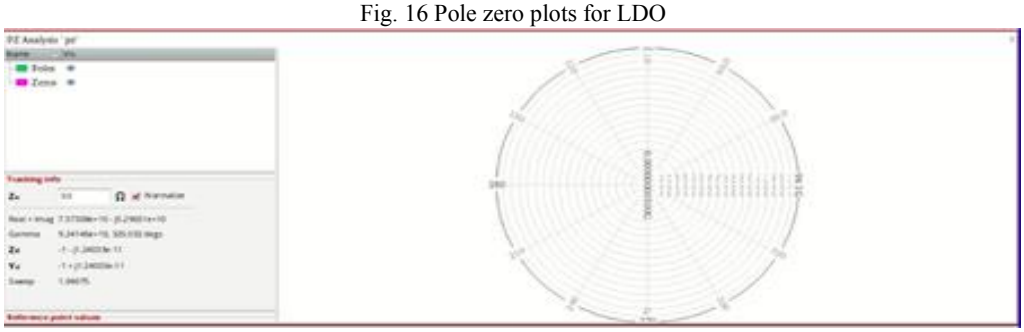

Fig. 17 Pole zero location in S-plane for LDO

C. *Line Regulation*

Line regulation is the ratio of change in output regulated voltage to input voltage, and the simulated results are given in Fig. 18 and 19 for regulated voltages of 850mV and 1.35V, respectively. The relevant output and input values are presented in the next case study including the simulation results.

Case (1): LDO tuned to show a regulated constant output voltage of 850mV.

To tune the LDO to have a controlled output voltage of 850mV, the resistors R_1 and R_2 on the output side are configured to have values of 6 and 844, respectively. The load regulation of LDO can be seen by adjusting the load resistor RL. The shift in the regulated output voltage relative to the input voltage is known as line regulation. As shown in Fig. 18 the regulated voltage is 850mV. The corresponding values of output and input values are shown in the Table IV.

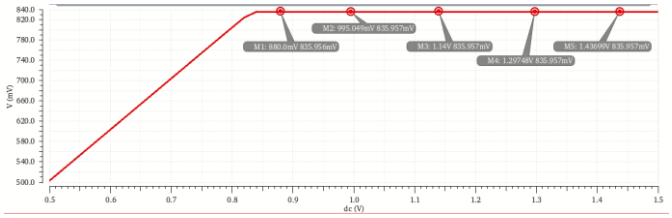

Fig. 18 Variation of Vout with Vin for 850mV regulated voltage

TABLE IV. VOUT VS VIN WHEN LDO TUNED AT 0.85V REGULATED VOLTAGE

V_{in} (V)	V_{out} (mV)
0.8501	879.8568
0.940	879.8629
1.046	879.8630
1.2041	879.8630
1.32	879.8630
1.446	879.8630

Case (2): LDO tuned to show a regulated constant output voltage of 1.35V.

The resistors R_1 and R_2 at the output side of the LDO is designed to have values 356Ω and 844Ω respectively to tune the LDO to have a regulated output voltage of 1.3V. By varying load resistor RL the load regulation of LDO can be seen. Line regulation is defined as the change of the regulated output voltage relative to the input voltage. As shown in Fig. 19 the regulated voltage is 1.35V. The corresponding values of output and input values are shown in the Table V.

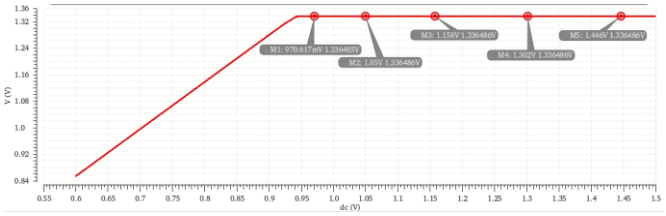

Fig. 19 Variation of Vout with Vin for 1.35V regulated voltage

TABLE V. VOUT VS VIN WHEN LDO TUNED AT 1.35V REGULATED VOLTAGE

V_{in} (V)	V_{out} (mV)
0.860	1.336840
0.896	1.336956
1.014	1.336957
1.145	1.336957
1.302	1.336957
1.456	1.336957

In order to evaluate the required characteristic parameter of LDO equations 14, 15, 16 & 17 are used:

Dropout voltage $$V_{drop} = V_{in} - V_{out} \quad (14)$$

Quiescent current $$I_q = I_{in} - I_{out} \quad (15)$$

Current efficiency $$E_i = \frac{I_{out}}{I_{in}} \quad (16)$$

Efficinecy of LDO $$= \frac{I_{out} V_{out}}{(I_{out} + I_q) V_i} * 100 \quad (17)$$

Table VI compares the proposed LDO regulator against various earlier publications in terms of performance. Although the Efficiency of LDO is less than that of the proposed work, the proposed LDO regulator benefits from superior performance in output variations and current efficiency. The current efficiency is increased, and quiescent current is decreased to a very less value.

VI. RESULTS AND DISCUSSIONS

In this proposed work, a highly robust capacitor-less-low-dropout (OCL-LDO) regulator has been implemented in a standard 90nm CMOS technology, taking into account the need for an energy efficient and stable LDO regulator. Unlike the traditional regulators, the proposed circuit was designed to provide 1.2V output-voltage at an output-current of 100mA even when input voltage is greater than 1.35V. This is the only proposed LDO regulator with two stage error-amplifier for higher stability of 70deg. The table VII shows the performance comparison of the proposed LDO with that of the previous works 100mA output current. First the proposed LDO has the lowest quiescent current of 0.02µA which is the lowest compared to other works, secondly the current efficiency achieved is the highest among the compared LDO regulators, the stability analysis also shows that the phase margin is 70.636deg and is the most and best stable regulator.

Next the total power dissipation for the same output current is only 0.2mW which is the lowest compared to the previous works. Finally, the dropout voltage of the proposed work is 100mV whereas other works are more than 100mV. The figure of merit of the proposed regulator is competitive in terms of power, quiescent current, efficiency, and stability. The very important component that is crucial stable output regulated voltage in a LDO regulator is the BGR, very important component that is crucial stable output regulated voltage in a LDO regulator is the BGR, the reference voltage is derived from BGR to LDO due to this reason the rise time of the output current is very small and reaches maximum of 100mA, to have wide temperature range operation of LDO the BGR circuit is suitable from -25°C to 120°C and is stable , the total power usage is very low hence called low power consumption regulator the reference voltage is derived from BGR to LDO due to this reason the rise time of the output current is very small and reaches maximum of 100mA,to have wide temperature range operation of LDO. The BGR circuit is suitable for low power and is stable; the total power usage is very low hence called low power consumption regulator. The experimental results obtained by the proposed regulator are comparable and are especially encouraging, these features are very important for analog sensing applications.

TABLE VI. PERFORMANCE SUMMARY AND COMPARISON WITH EXISTING WORK

Design Parameters	[3]	[5]	[6]	[12]	[18]	This work
Technology (CMOS)	90nm	180nm BCD	180nm	90nm	180nm	90nm
VIN/VOUT(V)	1/0.8	5/5.25	1.8/1.688	1.2/1	1.8/1.66	1.2
Load capacitor CL(µF)	1	2.2	-	0.1	40p	0
Maximum IQ(µA)	60	35.6	4.41	26	1.5	0.02
Maximum Iout(mA)	100	250	50	-	100	100
Current efficiency (%)	99.94	-	93	-	99.89	99.99
Efficiency of LDO (%)	83.94	-	93	-	-	91.72
Phase Margin (No-load) (deg)	-	-	-	-	-	64.516
Phase Margin (Full-load) (deg)	-	-	63	-	-	70.635
Power dissipated (mW)	7.5	-	0.387	-	-	0.2
Dropout voltage(mV)	200	250	120	200	200	100

VII. Conclusion

This study describes a 90nm CMOS-based ultra-low quiescent current, low-dropout- regulator. BGR provides added feature like temperature-independent, regulated LDO-output. These benefits allow the proposed regulator to operate in a wide variety of operating circumstances, with a current efficiency of 99.99 percent and a quiescent- output- current of 0.02 A. The indicated LDO has a high level of stability, with a phase margin of 64.516deg without load and 70.63deg with load, power supply noise rejection is improved by use of large dc gain op-amp of 50dB it can also be used to produce steady voltages in the 0.85V to 1.35V range without the use of a bulky off-chip capacitor on the output side. BGR circuit is suitable from -25°C to 120°C and is stable; the total power usage is very low hence called low power consumption regulator with 0.2mW and due to these reasons the BGR based LDO can be used as constant source voltages for devices that work in deep submicron innovation with very low voltages less than 1.2V.

References

[1] J. Hu and M. Ismail, "A true zero-load stable CMOS capacitor-free low dropout regulator with excessive gain reduction," in Proc. IEEE Int. Conf. Electron. Circuits Syst. (ICECS), Dec. 2010, pp. 978–981.

[2] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed. John Wiley & Sons, Inc., 2001.

[3] Huang, Chung-Hsun, Ying-Ting Ma, and Wei-Chen Liao."Design of a low-voltage low-dropout regulator", IEEE transactions on very large-scale integration (VLSI) systems 22.6(2013):1308-1313.

[4] Tan, Yi, Chenchang Zhan, and Guanhua Wang. "A Fully-On-Chip Analog Low-Dropout Regulator with Negative Charge Pump for Low-Voltage Applications." IEEE Transactions on Circuits and Systems II: Express Briefs 66.8(2018):1361-1365.

[5] Joshi, Kishan, Sanjeev Manandhar, and Bertan Bakkaloglu. "A 5.6 μ A Wide Bandwidth, High Power Supply Rejection Linear Low-Dropout Regulator With 68dB of PSR Up To 2 MHz." IEEE Journal of Solid-State Circuits (2020).

[6] Bautista, Meriam Gay, et al. "Design of low power, high PSRR low drop-out voltage regulator." 2015 International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment and Management (HNICEM). IEEE, 2015.

[7] Motkurwar, Supriya, and Ujwala Ghodeswar. "Design and power noise cancellation analysis of low dropout voltage regulator." 2016 International Conference on Communication and Signal Processing (ICCSP).IEEE, 2016.

[8] Alapati, Suresh, and Sreehari Rao Patri. "Improved transient response capacitor less low dropout regulator employing adaptive bias and bulk modulation." Turkish Journal of Electrical Engineering & Computer Sciences 26, no.5 (2018):2385-2394.

[9] Madhukumar AS, M. Nagabhushan,"Design and Implementation of less quiescent current, less drop out LDO Regulator in 90nm Technology", International Journal of Engineering Trends and Technology (IJETT) – Volume 23Number 8-May 2015.

[10] Y. Hwang, M. Lin, B. Hwang, and J. Chen, "A 0.35μm CMOS sub-1v low quiescent- current low-dropout regulator," in Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC), 2008, pp. 153–156.

[11] Hu, John, Brian Hu, Yanli Fan, and Mohammed Ismail. "A 500nA quiescent, 100 mA maximum load CMOS low-dropout regulator", In 2011 18th IEEE International Conference on Electronics, Circuits, and Systems, pp. 386-389.IEEE,2011.

[12] Akhamal, Hicham, MostafaChakir, and Hassan Qjidaa. "A 90nm CMOS «LDO» regulator with high load regulation using a gain boost-up technique." 2016 5th International Conference on Multimedia Computing and Systems (ICMCS), IEEE, 2016.

[13] R. Magod, N. Suda, V. Ivanov, R. Balasingam, and B. Bakkaloglu, "A 14.8μV RMS integrated noise output capacitor-less low dropout regulator with a switched-RC bandgap reference," in Proc. IEEE Custom Integr. Circuits Conf. (CICC), Sep. 2015, pp. 1–4.

[14] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," IEEE J. Solid- State Circuits, vol. 45, no. 3, pp. 565–577, Mar. 2010.

[15] Tewari, Shikhar, and Kirmender Singh."Intuitive design of PTAT and CTAT circuits for MOSFET based temperature sensor using Inversion Coefficient based approach."In201519th International Symposium on VLSI Design and Test, pp. 1-6, IEEE, 2015.

[16] G. Balachandran and R. Barnett, "A 110 nA voltage regulator system with dynamic bandwidth boosting for rfid systems," IEEE J. Solid-State Circuits, vol. 41, no. 9, pp. 2019–2028, 2006.

[17] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," IEEE J. Solid-State Circuits, vol. 42, no. 8, pp. 1732–1742, Aug. 2007.

[18] Peng, Sheng-Yu, Li-HanLiu, Pei-KeChang, Tzu-YunWang, and Hao-Yu Li. "A power-efficient reconfigurable output-capacitor-less low-drop-out regulator for low-power analog sensing front-end." IEEE Transactions on Circuits and Systems I: Regular Papers 64, no.6(2017):1318-1327.

[19] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS," in Proc. IEEE Custom Integrated Circuits Conf. (CICC), 2010, pp. 1–4.

[20] Lai, Suming, and PengLi."A power-efficient on-chip linear regulator assisted by switched capacitors for fast transient regulation", International Symposium on Quality Electronic Design (ISQED). IEEE, 2013.

PAVAN M S obtained his graduation in BE, Electronics & Communication Engineering from VidyaVardhaka College of Engineering, Mysore in 2018 and is currently pursuing M.Tech in VLSI and Embedded Systems at Ramaiah Institute of Technology, Bangalore.

M. NAGABUSHANAM obtained his B.E. degree from Bangalore University in Electronics Engineering in 1997, M.Tech in Electronics Engineering from Visvesvaraya Technological University in 2003 & obtained Ph.D in VLSI from Anna University, Chennai in 2017. He joined Department of Electronics & Communication Engineering, M.S. Ramaiah Institute of Technology in 2003 as Assistant Professor. He has over 19 years of teaching experience in Analog Electronics, VLSI, and Advanced mixed signal design, linear integrated circuits. Microelectronics, CMOS VLSI design, solid state devices, optical fiber communications. His area of specialization is VLSI, Image processing, mixed signal design. He is a recognized reviewer for few reputed journals and has published more than 25 research papers in National and International Journals. He is also a visiting professor at Manipal University, Bangalore University, Birla institute of technology & science. He is a life member ISTE since 2010 and member IAENG since 2019.

SUSHMITA HAWALDAR obtained her graduation in BE, Electronics & Communication Engineering from Basaveshwar Engineering College, Bagalkot in 2017 and is currently pursuing M.Tech in VLSI and Embedded Systems at Ramaiah Institute of Technology, Bangalore.

GANGADHARAIAH S. L completed B.E. in Electronics and Communication Engineering from Kuvempu University in 1997, M. Tech in Digital Electronics and Advanced Communication from KREC, Surathkal in 2002. Currently, he is pursuing Ph.D in the area of VLSI signal processing under VTU, Belgaum. Presently he is working as Assistant Professor in the Department of Electronics & Communication Engineering, M. S Ramaiah Institute of Technology, Bengaluru, since 2002. His areas of interest are Analog VLSI, Digital VLSI, VLSI Signal Processing and Machine Learning.

Contribution of individual authors to the creation of a scientific article (ghostwriting policy)

Author Contributions: Please, indicate the role and the contribution of each author:
Pavan M S. proposed the LDO regulator in 90nm CMOS Technology and designed the complete circuit.
Dr. M. Nagabushanam guided, directed with required specifications for the design of LDO regulator in 90nm CMOS Technology and proposed the stability analysis.
Sushmita Hawaldar did the study on regulators and carried out simulation, executed and prepared original draft.
Gangadharaiah. S. L. was involved in reducing bottlenecks in design during simulation and also responsible for editing the research article.

Sources of funding for research presented in a scientific article or scientific article itself
No source of funding