Novel Static Ultra Low-Voltage and High Speed CMOS Boolean Gates

Yngvar Berg and Omid Mirmotahari

***Abstract*— In this paper we present robust and high performance static ultra low-voltage CMOS binary logic. The delay of the ultra low-voltage logic presented are less than 10% of the delay of standard CMOS inverters. The logic gates presented are designed using semi floating-gate transistors and a current boost technique. The boolean gates resemble domino CMOS. The performance and robustness of different logic gates are examined and compared to complementary and domino CMOS logic.**

***Index Terms*— CMOS, Low-Voltage, Domino logic, Floating-Gate, High-Speed, NAND, NOR.**

I. Introduction

The need for novel digital logic styles for both ultra low supply voltage and low power applications is more and more evident. Especially, for hand held and mobile equipement, the power and supply voltage are important aspects to consider when designing both analog and digital systems. The digital circuits shrink rapidly with the introduction of recent semiconductor processes. The energy requirement for switching digital signals are at its minimum when the supply voltage is at its minimum[1]. However, the performance og digital systems is often characterized by Energy-Delay-Produc (EDP) which for most applications will entail a optimum for supply voltages close to the threshold voltage of the transistors used. Low supply voltage can be a requirement as a result from a power reduction strategy in digital circuitry.

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) and Low-Power (LP) logic [2]. However, in modern CMOS technologies there are significant gate leakage which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom [2]. There are several approaches to FG CMOS logic [3], [4], [5], [6]. The gates proposed in this paper are influenced by ULV non-volatile FG circuits [7]. The logic style characterized in this paper is based on dynamic and static ULV inverters presented in [8], [9], [10], [11]. The semi-floating gates utilized in this paper have been expoided in low-voltage high speed Flip-Flops [12]. In section 2 the static ULV differential domino inverter is described followed by a differential static ULV NAND and NOR gates in section 3.

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II. Static ULV Logic

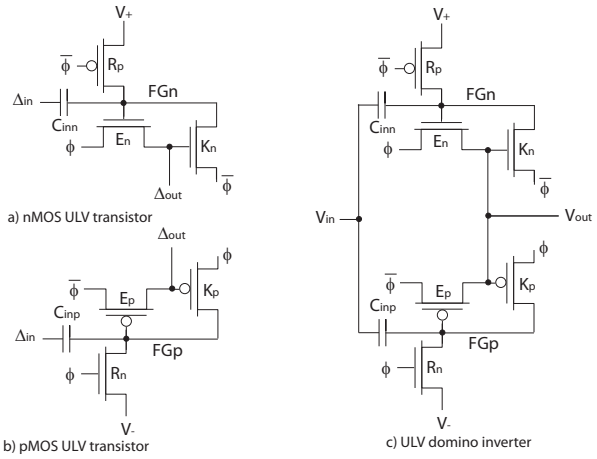

Fig. 1. *a) nMOS ULV transistor, b) pMOS ULV transistor and c) static ultra low-voltage semi-floating-gate recharge inverter. The transistors labeled K_n and K_p provide a feedback making the output static.*

The ULV transistor configurations and an ULV domino inverter is shown in Figure 1. The ULV transistor configuration consists of two three standard transistors:

- **Evaluate transistor**, E_p or E_n. The evaluate transistors are driving the gate outputs.
- **Recharge transistor**, R_p or R_n. The recharge transistors are used to recharge the gate of the evaluate transistors in the precharge mode.
- **Keeper transistor**, K_p or K_n. The keeper transistors are used to reduce the static current consumption by draining one of the evaluate transistors in the evaluation mode. The keeper transistors will improve both power consumption and noise margin.

The static ULV domino inverter[9] shown in Figure 1 c) will be precharged to $V_{DD}/2$ in the precharge phase and invert any input changes occuring in the evaluation phase, i.e. $\Delta V_{out} = -\Delta V_{in} \equiv |V_{DD}/2|$.

The recharge and evaluation mode are characterized by:

- **Precharge/recharge**, shown in Figure 2 a). The nMOS floating-gate is recharged to V_+ and the pMOS floating-gate is recharged to V_- while the output and input are precharged to $V_{DD}/2 = (V_+ - V_-)/2$. The output will be forced to $V_{DD}/2$ due to a reversed biased inverter.
- **Evaluate**, shown in Figure 2 b). The output will be pulled to V_{DD} if a negative transition, $\Delta V_{in} = -V_{DD}/2$, occurs and to V_{SS} if there is a positive transition, $\Delta V_{in} = V_{DD}/2$, applied at the input.

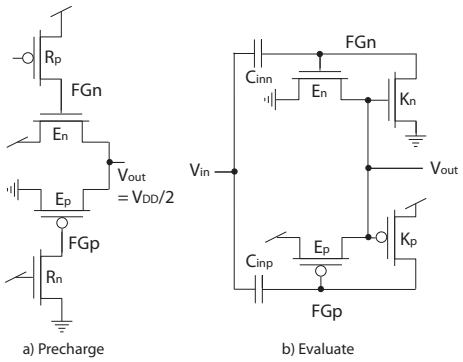

Fig. 2. *a) ULV inverter in precharge mode and b) ULV inverter in evaluate mode.*

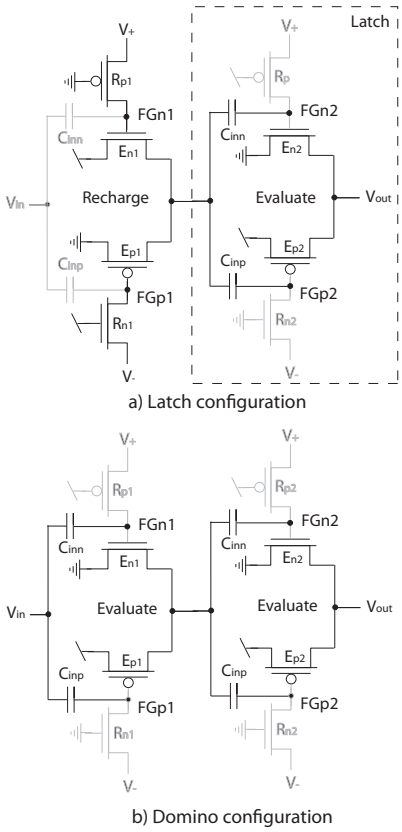

Fig. 3. *Simpel ULV Inverter, a) latch configuration and b) domino configuration.*

Domino and latch configurations of the simple ULV logic are shown in Fig. 3. The clock signals are used to provide virtual references in recharge/precharge and evaluate mode in addition to turning on and off the recharge transistors.

The current drawn by the inverter providing the virtual reference, shown in Fig. 4, is equal to the ON current of the evaluate transistors E_n or E_p. In this case the inverter providing the ϕ signal is not sufficiently strong to pull the virtual ground to $0V$ and the static current drawn by the ULV inverter is approximately $10nA$. In order to reduce the static current the floating-gate of the pMOS evaluate transistor must be raised to V_{DD}. By doing this the current running through the transistor is reduced to the off current of a complementary

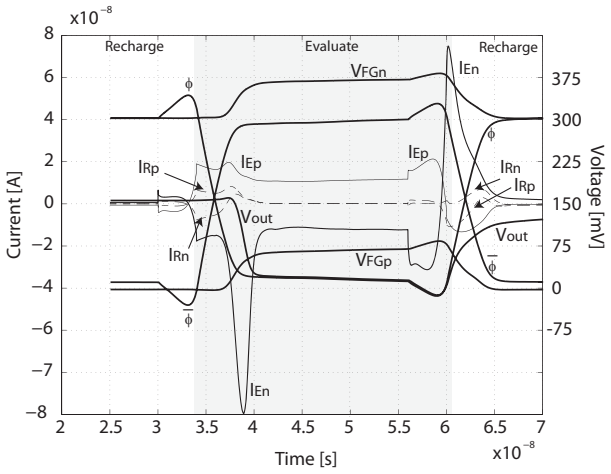

Fig. 4. *The response of the ULV inverter. The supply voltage is* $300mV$

inverter and both the output and the virtual ground, i.e. ϕ are drawn closer to ground (0V). The output is pulled down to the virtual ground by a large current provided by the E_n transistor. The fall time of the ULV inverter is significantly less than the fall time of ϕ due to the biased transistor. The input may be an ULV gate operating in the same phase, i.e. domino, or an ULV gate operating in the opposite phase, i.e. latch. In order to implement fast latches the transient to $V_{DD}/2$ needs to be fast as well. Note that the simple ULV latch is quasi-static because the precharge input signal will force the output of the latch to one of the rails. The input signal is locked to $V_{DD}/2$ for the rest of the clock phase and hence the input can not affect the latch. Any leakage affecting the latch will not yield a sharp transient.

In the start of the recharge phase, shown in Fig. 4, the output is close to one of the virtual references. Assume that the nMOS evaluate transistor E_n is ON with an effective gate voltage $V_{FGn} = V_+ + k \cdot V_{DD}/2 - V_{out}$ where $k = C_{inn}/C_T$ and C_T is the total capacitance seen by the nMOS floating gate. The output is assumed to be 0V (GND) in this case. Initially the large current will pull the output quickly towards $V_{DD}/2$, i.e. the output will follow the sharp clock edge. As the clock signals starts to switch the ϕ will increase and provide a positive current into the output while the $\overline{\phi}$ will decrease and contribute with a positive current into the output node as long as $V_{\overline{\phi}} > V_{out}$. This current will contribute in pulling the $\overline{\phi}$ clock signal down to 0. In this way the current running through the E_p transistor will not contribute to the power consumption. When the output is approaching V_{DD}, assuming that $\phi \approx 1$ and $\overline{\phi} \approx 0$, the currents running through the evaluate transistors will be very small due to the effective voltage $V_{FGn} \approx V_+ - V_{DD}/2$. As can be seen in Fig. 4 the delay of the ULV gate in domino configuration is significantly less than the recharge delay of the same gate and hence the delay from the recharge crossing $V_{DD}/4$ through two domino ULV gates is negative. The ULV gates in evaluation mode will respond to the initial recharge of the preceding ULV gate. For a supply voltage equal to $300mV$ the delay from the clock edge through a latch and a ULV domino inverter is $1.17ns$

whereas the delay through two ULV domino gates is $0.56ns$.

A. Differential Static ULV Logic

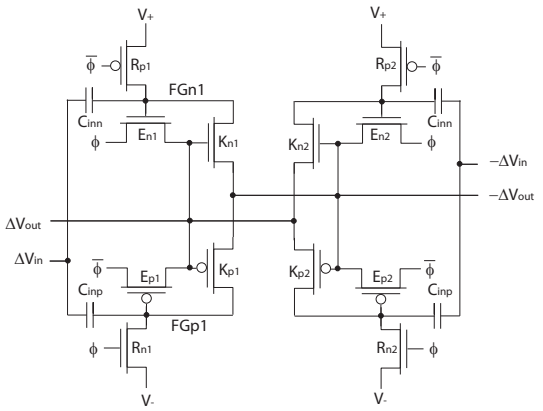

Fig. 5. *Differential ULV inverter (DSULV).*

A problem with the SULV logic is the potential false output transient if the input transient is significantly delayed compared to the clock edge. If the output reaches a false state the state will be fixed. By using a differential ULV style shown in Figure 5 the keepers will not be activated before the arrival of the input transient.

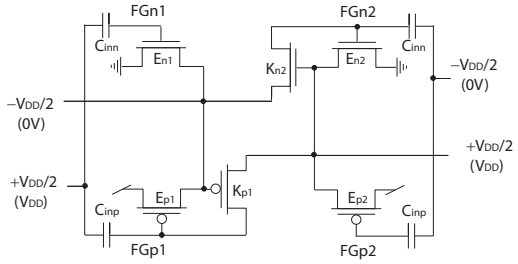

Fig. 6. *Differential ULV inverter in evaluate mode assuming an input* $\Delta V_{in} = V_{DD}/2$.

The differential ULV inverter in evaluation mode is shown in Figure 6 assuming $\Delta V_{in} = V_{DD}/2$.

III. ULV NAND/NOR GATES

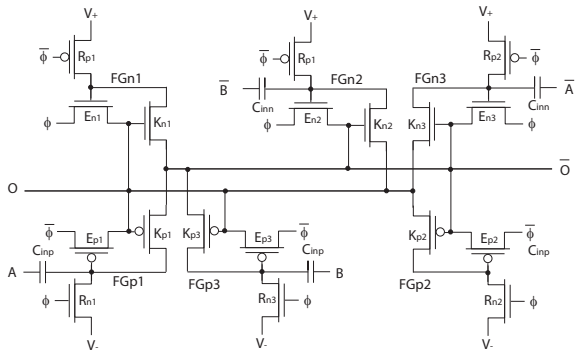

Fig. 7. *Differential ULV NAND gate (N1).*

	C_L	E_{n1} V_{eff}	E_{p2} V_{eff}	V_{gs} I_{LEAK}	NM^*
N1	14C	V_{DD}	V_{DD}	V_{DD}	V_{DD}
N2	17C	$\frac{3V_{DD}}{2}$	$\lvert\frac{3V_{DD}}{2}\rvert$	$\frac{4V_{DD}}{3}$	$\frac{3V_{DD}}{2}$

TABLE II

Worst case, ie.e $A = B = 1/2$ *for N1 and* $A \neq B$ *for N2.*

The differential ULV NAND (N1) gate is shown in Figure 7. By applying the two inputs A and B to two parallel static pMOS ULV transistors, the output O will be pulled from $V_{DD}/2$ (1/2) to V_{DD} (1) if any of the these inputs swiches from 1/2 to 0. Assuming that the external load for each output is $C_{inn} + C_{inp} \approx 6C$, yielding a capacitive division factor fot the floating capacitances equal to 1/2, we can derive a simple model for the output load of the gate; $C_L = C_{inn} + C_{inp} + 2C_d + 3C_g + 3C_s \approx 14C$. The delay of the NAND gate is dependent on the input signals, the delay increases with the number of positive input transients of A and B as shown in Table I. The worst case delay is obtained when $A = B = +1/2$ ($\overline{A} = \overline{B} = -1/2$) because the current level of nMOS evaluate transistor E_{n1} is not increased. The response of the gate will be correct due to the decrease in current level of both E_{p1} and E_{p3}. The synchronization of the input signals is important for the NAND gate shown in Figure 7. Consider the case where the one of the input signals is delayed compared to the other input signal. If the first arriving input transient is $+1/2$, for example $A = +1/2$ and $\overline{A} = -1/2$, the current level of transistors E_{p1} and E_{n3} will be reduced and transistor E_{n1} will pull output 0 down towards 0 (gnd) while E_{p2} will pull $\overline{O}$ towards 1. The current levels of E_{p3} and E_{n2} will not be reduced significantly until the keeper transistors K_{p3} and K_{n2} kicks inn. The timing response of the NAND gate in this stutation is dependent the diffence in driving capabilites of transistor E_{n1} and E_{p3}, and E_{p2} and E_{n3}. We may assume that the current providing a transient at B and $\overline{B}$ will be at least twice the current level pulling the outputs due to the leakage situation decribed. If the NAND gate snaps into a false state it will not be influenced by the second input and the false state will be crucial.

There are some additional problems associated with the NAND gate

1) The worst case delay. Determined by the inputs $A = B = -1/2$ yielding an effective gate voltage equal to V_{DD} of E_{n1} (and E_{p3}). The minimum ON current, i.e. effective gate voltage, should be as high as possible in order to reduce the delay and increase the noise margin.
2) The leakage current compared to the minimum ON current, both determined by an effective gate voltage equal to V_{DD}. The minimum ON current should be higher than the leakage current, i.e. higher effective gate voltage for the ON transistor.
3) The minimum ON current compared to the maximum ON current, given by effective gate voltages equal to V_{DD} and $\frac{3V_{DD}}{2}$. A large difference in ON currents will yield an increased power consumption.

In order to increase the worst case speed of the NAND gate

A	B	O	E_{p1}	E_{p3}	E_{n2}	E_{n3}	Speed
0 (-1/2)	0 (-1/2)	1 (1/2)	on	on	on	on	Fast
0 (-1/2)	1 (1/2)	1 (1/2)	on	off	off	on	Medium
1 (1/2)	0 (-1/2)	1 (1/2)	off	on	on	off	Medium
1 (1/2)	1 (1/2)	0 (-1/2)	off	off	off	off	Slow

TABLE I

The operation of the differential ULV NAND (N1)gate.

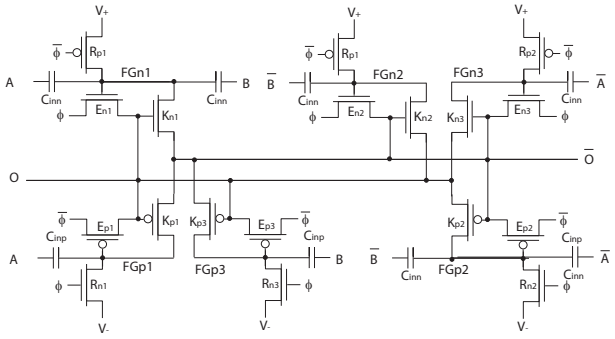

Fig. 8. *Differential ULV NAND (N2) gate.*

we can add floating input capacitors as shown in Figure 8 (N2). The timing response of the N2 gate is less dependent of the input signals and more similar to complementary CMOS. All evaluate transistors receive inputs and the current level in the worst case will be increased compared to N1. When $A = B = 1/2$ the effective voltage of E_{n1} is increased from V_{DD} to $\frac{3V_{DD}}{2}$ as shown in Table II. The worst case delay for N2 is when $A \neq B$ and the timimg response is not significantly dependent of the input values. Furthermore we can apply a simple model for the noise margin $NM = V_{ON}/V_{OFF} \approx V_{ON}$, where V_{ON} is the maximum current level of the evaluate transistors in the worst case, i.e. $A = B = 1/2$ for N1 and $A \neq B$ for N2, and $V_{OFF} = OV$ is the OFF current or static leakage current. The ON current of the ULV NAND2 gate is approximately 10 times the ON current of a complementary CMOS inverter while the OFF currents are equal. In effect this will increase the ratio of the ON to OFF current of the ULV gates compared to complementary CMOS. By inverting the inputs of the circuit shown in Figure 7 and 8 the boolean function is changed to NOR2. The performance of the NOR2 gates are equivalent to the NAND gates in terms of speed, power, EDP and robustness. Furthermoore, the UVL logic gates presented in this paper can easily be applied as latches by using two gates with opposite clock signals [9].

A. Simulation Results

The minimum, $A = B$, and the maximum, i.e. $A \neq B$, parasitic delay for the NAND (N2) ULV gate is shown in Table III and Figure 9. The effect of a natural load can easily be estimated. If the ULV NAND2 gate is driving a similar gate the addidional load will be $C_{inn} + C_{inp}$ which is an increase of the load equal to 75%. For a CMOS inverter the added load would be 100%. The proposed domino logic style can be used to reduce the delay in critical paths and in critical subcircuits

VDD	N2 min	N2 max	CMOS	Relative
200mV	3.31ns	5.39ns	14.01ns	38%
250mV	0.689ns	0.931ns	4.15ns	22%
300mV	0.264ns	0.426ns	1.63ns	26%
350mV	0.110ns	0.165ns	0.583ns	28%
400mV	0.058ns	0.082ns	0.292ns	28%

TABLE III

The minimum, $A = B$, and the maximum, i.e. $A \neq B$, parasitic delay for the NAND2 ULV gate. The parasitic delay for complementary CMOS inverter is also shown.

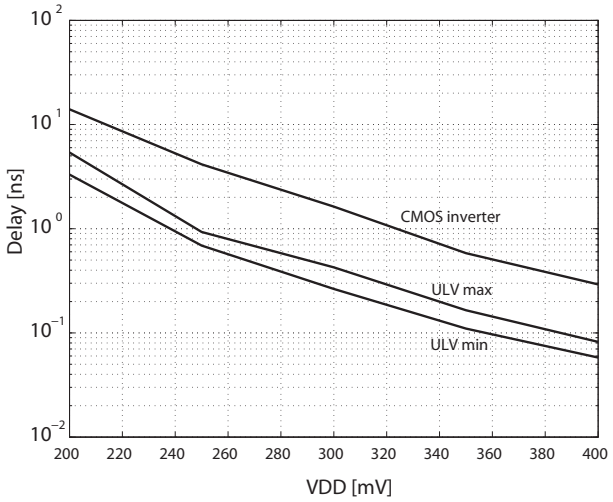

Fig. 9. *Maximum and minimum delay for the ULV differential NAND2 gate.*

and systems.

The response of the DSULV logic is shown in Fig. 10. The virtual supply voltages are very close to the references which yields an improved noise margin. The pMOS floating-gate V_{FGp} is drawn to V_{DD} by the pMOS keeper transistor K_p. The static current in the evaluation phase when the output is stable is reduced from $10nA$ to $50pA$.

The recharge delay, the delay through two ULV gates and total delay through an ULV latch and two ULV gates as function of the supply voltage is shown in Fig. 11. A critical delay path starts with a recharge delay and a numbe of domino delays. Compared to complementary CMOS the ULV logic delay is significantly reduced even for short domino paths. By adding keepers the ULV logic style becomes more robust.

The logic operation of the simple ULV and SULV logic styles are dependent on some critical timing properties as shown in TABLE IV. The problems becomes more severe

CLK	200	250	300	350	400	450	500	
Ideal	11	20	28	30	13	5	2	D
Norm	2	4	12	7	6	4	2	D
Ideal	5	12	28	69	313	926	2041	F
Norm	6	18	33	100	275	705	1471	F
Ideal	97.0	98.0	98.7	100	98.6	100	98.2	L
Norm	92.3	97.6	98.5	100	97.7	95.6	95.2	L

TABLE IV

Dynamic limitations for ULV and SULV logic for supply voltages in the range 200mV to 500mV. D is maximum logic depth for SULV, F (MHz) is minimum frequency for maximum logic depth for SULV and L is ouput level (%) for ULV logic.

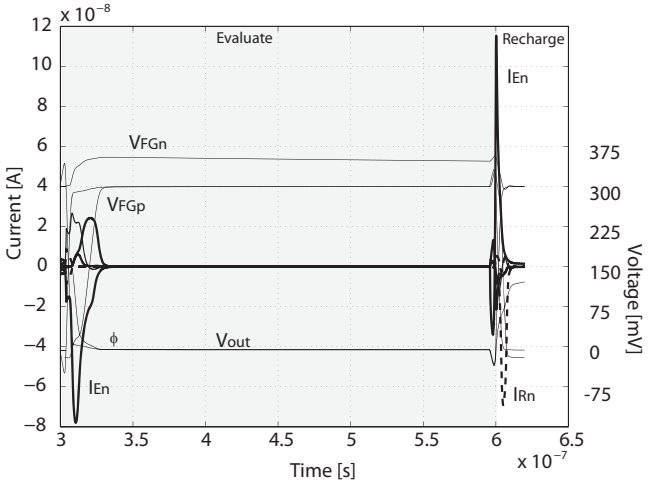

Fig. 10. *The response of the DSULV inverter. The supply voltage is* $300mV$.

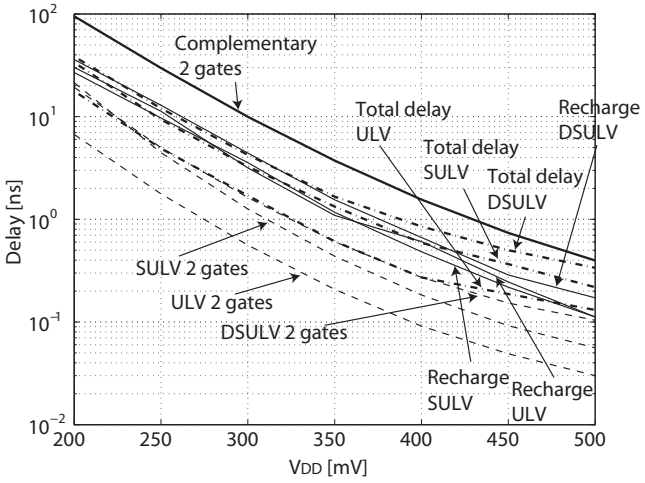

Fig. 11. *Recharge delay, the delay through two ULV gates and total delay through an ULV latch and two ULV gates.*

if the driving capability of clock drivers are reduced, i.e. inverters with transistor widths increased by four times (Norm) compared to minimum transistors used in the ULV gates. The delay through two gates for different logic styles for low supply voltages are shown in Fig. 12 and the delay of the ULV logic stales relative to complementary inverters are shown in Fig. 13. As expected the optimal supply voltage is close to the threshold voltage ($\approx 250mV$) of the transistors.

IV. Conclusion

Ultra low-voltage and high speed differential NAND and NOR gates have been presented. The gates offers increased speed and noise margin for ultra low-voltage applications. Preliminary simulation results are included for a $90nm$ CMOS process.

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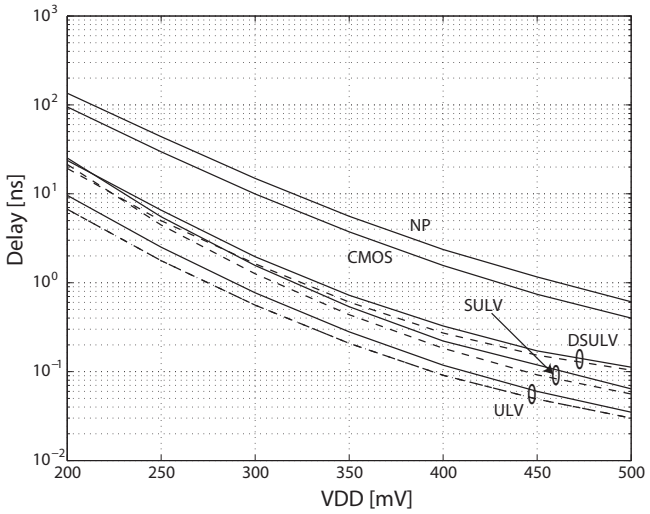

Fig. 12. *The delay through 2 inverters for different supply voltages.*

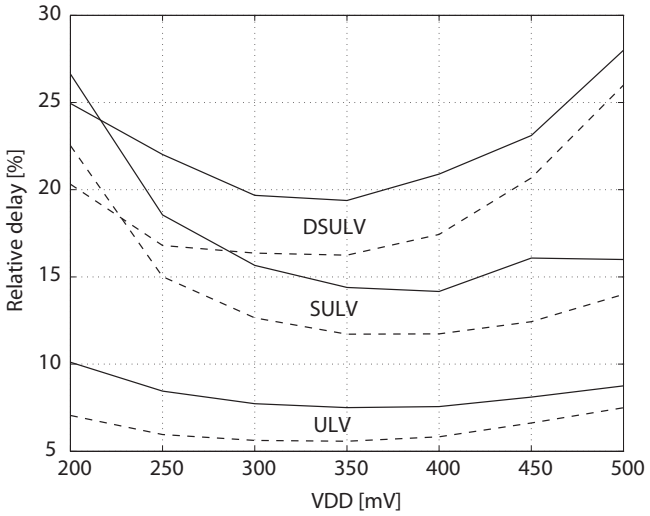

Fig. 13. *The relative delay through 2 inverters for different supply voltages. Solid lines represents relative delay assuming ideal clock signals and the dashed lines represents the relative delay assuming normal (Norm) clock drivers.*

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